 Apple Lisa Computer
Technical Information

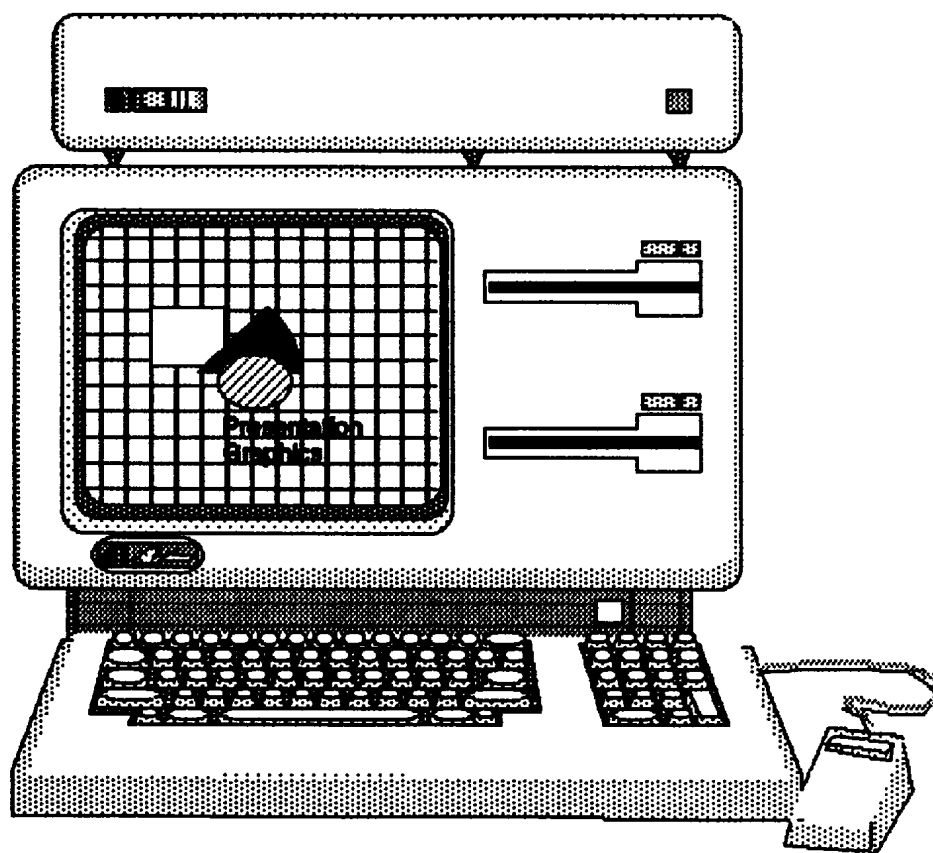# Apple Lisa Computer:
Hardware Manual
1983
(with Errata)

Lisa Computer:
1983 - 1985

Apple Lisa Personal Computer
1983 to 1985

Hardware
Manual (May 83)

MACINTOSH XL HARWARE INFORMATION UPDATE

Uploaded to CompuServe by Gary Kato

See also: **Lisa Hardware Manual**

Written by: Mark Baumwell (Apple Computer, Inc.)   16 May 1985

This document covers Macintosh XL information that is either incorrectly documented or not documented elsewhere.

I/O Space Addresses

The *Lisa Hardware Manual* shows incorrect addresses for locations in the I/O space such as the expansion slots, floppy disk controller, serial ports, parallel ports, keyboard/mouse control, etc. The addresses are listed as 00xxxx in the manual, but should be FCxxxx. As an example, refer to Figure 2-6 (System I/O Space Overview) in the Lisa Hardware Manual. The correct addresses for the expansion slots are (all in hexadecimal):

Addresses	Function
FC0000 - FC1FFF	Expansion slot # 1 Low Decode
FC2000 - FC3FFF	Expansion slot # 1 High Decode
FC4000 - FC5FFF	Expansion slot #2 Low Decode
FC6000 - FC7FFF	Expansion slot #2 High Decode
FC8000 - FC9FFF	Expansion slot #3 Low Decode
FCC000 - FCBFFF	Expansion slot #3 High Decode

Also note that while the I/O space addresses are in the range FCxxxx, the Boot ROM addresses are in the range FExxxx.

{ Actually that's Figure 2-5. - gary - }

Reading the Boot ROM version number
To check the version number of the Boot ROM, display location FE3FFC for 4 bytes. If you display it from LisaBug, the display looks something like this:

        00FE3FFC 0248

LISA: Lisa Hardware Information   1

The version number is 0248, or 2.48. Note that 48 hex = ASCII H. Therefore the ROM revision is H. Note the Boot ROM version number and the Floppy ROM version number are displayed in the upper right hand corner of the Macintosh XL screen during the self test. For example if H/88 was displayed on the screen during the self test, the Boot ROM is revision H and the Floppy ROM version is 88.

Reading Parallel Interface Card ROM Version Numbers

Note that if a Parallel Interface Card is installed, you can check its ROM version number by adding FF8 to the start of the Low Decode address of the slot the card is in and then displaying the resulting 4 bytes. To interpret the version number, look at the low order byte of each word. For example, to check the ROM version number of a Parallel Interface Card in slot 2, display location FC4FF8 for 4 bytes. If you display it from LisaBug, the display looks something like this:

        00FC4FF8   0001 0007

Since the ROM is on the lower half of the data bus, the upper half of the data bus should be interpreted as don't cares. Therrefore, the version number is 0107, or 1.07.

Parallel Interface Card VIA Offsets

Each Parallel Interface Card has two 6522 Versatile Interface Adapters (VIAs), one for each parallel port. The address of the VIAs is found by adding constants to the Expansion slot decodes as described below.

 Add 2000 hex to the slot low decode to get the lower VIA base address.
 Add 2800 hex to the slot low decode to get the upper VIA base address.

 For example:

 FC2000 is the slot 1 lower VIA base address.
 FC2800 is the slot 1 upper VIA base address.

Internal VIA locations

There are two VIAs on the Macintosh XL I/O board. The first VIA (VIA1) is controlled by a COPS processor and is connected to the mouse, keyboard, and other peripherals. The second VIA (VIA2) controls the built-in parallel port. The VIA locations and offsets to their registers and timers are as follows:

```
VIA1BASE        .EQU    $FCDD81         ;Base address - offsets follow
ORB1            .EQU    $0              ;Port B output register
ORA1            .EQU    $2              ;Port A output register
DDRB1           .EQU    $4              ;Port B Data Direction register
DDRA1           .EQU    $6              ;Port A Data Direction register
T1LL1           .EQU    $C              ;Low Order T1 Latch
T1LH1           .EQU    $E              ;High Order T1 Latch
T2CL1           .EQU    $10             ;Low Order T2 Counter
T2CH1           .EQU    $12             ;Low Order T2 Counter

VIA2BASE        .EQU    $FCD901         ;Base address - offsets follow
ORB2            .EQU    $0              ;Port B output register
IRB2            .EQU    $0              ;Port B input register
ORA2            .EQU    $8              ;Port A output register
IRA2            .EQU    $8              ;Port A input register
DDRB2           .EQU    $10             ;Port B Data Direction register
DDRA2           .EQU    $18             ;Port A Data Direction register
T1LL2           .EQU    $30             ;Low Order T1 Latch
T1LH2           .EQU    $38             ;High Order T1 Latch
T2CL2           .EQU    $40             ;Low Order T2 Counter
T2CH2           .EQU    $48             ;Low Order T2 Counter
```

{ End of document - gary - }

Macintosh XL Hardware Information

See also: Lisa Hardware Manual (MAY 1983)

Written by: Mark Baumwell   16 May 1985

This document covers Macintosh XL information that is either incorrectly documented or not documented elsewhere.

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FCA000 - FCBFFF	Expansion slot #3 High Decode

Also note that while the I/O space adresses are in the range FCxxxx, the Boot ROM addresses are in the range FExxxx. (16K Rom)

Reading the Boot ROM version number

To check the version number of the Boot ROM, display location FE3FFC for 4 bytes. If you display it from LisaBug, the display looks something like this:

        00FE3FFC   0248

The version number is 0248, or 2.48. Note that 48 hex = ASCII H. Therefore, the ROM revision is H. Note the the Boot ROM version number and the Floppy ROM version number are displayed in the upper right hand corner of the Macintosh XL screen during the self test. For example if H/88 was displayed on the screen during the self test, the Boot ROM is revision H and the floppy ROM version number is 88.

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T1LL1           .EQU        $C              ; Low Order T1 Latch
T1LH1           .EQU        $E              ; High Order T1 Latch
T2CL1           .EQU        $10             ; Low Order T2 Counter
T2CH1           .EQU        $12             ; High Order T2 Counter
```

```
VIA2BASE        .EQU        $FCD901        ; Base address - offsets follow
ORB2            .EQU        $0             ; Port B output Register
IRB2            .EQU        $0             ; Port B input Register
ORA2            .EQU        $8             ; Port A Output Register
IRA2            .EQU        $8             ; Port A Input Register
DDRB2           .EQU        $10            ; Port B Data Direction Register
DDRA2           .EQU        $18            ; Port A Data Direction Register
T1LL2           .EQU        $30            ; Low Order T1 Latch
T1LH2           .EQU        $38            ; High Order T1 Latch
T2CL2           .EQU        $40            ; Low Order T2 Counter
T2CH2           .EQU        $48            ; High Order T2 Counter
```

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{Received by DTC of P Cubed: 6-Mar-1985}   *Pages: 326*

To: Readers   From: Gail Pilkington

Re: Lisa Theory of Operations   Date: June 3, 1983

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This memo covers the latest revision of the manuscript for the manuals
titled *Lisa Theory of Operations* (LTOO) and *Lisa Hardware Manual* (LHM).
The LHM includes:

o Chapters 1, 2, and 3 only,
o Condensed Preface
o No appendixes.

The LTOO manual will include everything in the version before you,
schematics in the appendixes, and a complete index.

Background

The manuscript was written by a consultant and reviewed by Paul Baker and
others. I edited the files to correct the errors and omissions,
eliminate ambiguous and inconsistent terminology, and generally clean
things up. I used an indented-outline format, which will not be used for
the final books, and I added space in the manuscript for line-art, wrote a
table of contents, and compiled this version. Time was not spent
preparing an index for this draft because it would not be correct for the
final books, which will be printed very soon.

The art in this version is the original art, which I hand-edited; line-art
will be produced by a consulting firm: CBM. In this manuscript, line-art
is not embedded. Instead, a page that provides space for line-art and the
figure caption is labeled with an "a" and the original art appears on a
separate page labeled "b"; see the table of contents.

Notations in this manuscript

Because the manuscript is written in Pascal, some special notations appear
in the text as an instruction to either the typesetter or, should we decide
not to typeset the books, to the person who uses LisaWrite to produce
camera-ready copy. Following are definitions and examples of the notations,
and examples of how the notations will look in the finished books.

1. Over bar: A slash mark followed by a space represents a bar over
    preceeding characters. For example, VMA/ becomes $\overline{\text{VMA}}$, B/L/ becomes
    $\overline{\text{B/L}}$, etc.

2. Binary, Hex, and Base 10: @2, @16, and @10 represent a subscripted 2,
    10, or 16. For example, FF@16 becomes FF_{16}, 00E010@16 becomes
    $00E010_{16}$, etc.

3. Multiplication sign: An exclamation point followed by a period, (!.),
    represents a raised multiplication sign. For example,
    SLOT/!.A20/!.A19 becomes SLOT/·A20/·A19
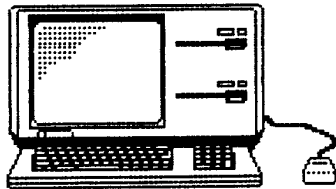
Apple Lisa Computer
1983 - 1985

Lisa Theory of Operations

WARNING: This equipment has been certified to comply with the
limits for a Class B computing device, pursuant to Subpart J
of Part 15 of FCC rules. Only peripherals (computer
input/output devices, terminals, printers, and the like)
certified to comply with the Class B limits may be attached to
this computer. Operation with noncertified peripherals is
likely to result in interference to radio and TV reception.

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CONTENTS

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PREFACE [condensed version]

The Lisa Hardware Manual provides information on the functional performance and general specifications of the Lisa. Chapter 1 provides a general introduction to the Lisa and gives a brief description of the architecture.

Chapter 2 is of interest to programmers who need to know the address and interrupt structure, as well as the operation of the memory mapping unit. Chapter 3 provides dimensions, environmental requirements, and interfaces that are useful to design engineers wishing to interface to the Lisa.

Following are other manuals that relate to the Lisa.

    o Lisa Owner's Guide

    o Lisa Theory of Operations

    o Profile Owner's Manual

    o Operating System Reference Manual for the Lisa.

    o Lisa Repair Manual (provided to dealer service departments)

xiii

PREFACE [expanded version]

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The Lisa Theory of Operations manual provides a detailed
description of the functional operation of the Lisa hardware.
Chapter 1 provides a general introduction to the Lisa and
gives a brief description of the architecture.

Chapter 2 is of interest to programmers who need to know the
address and interrupt structure, and the operation of the
memory mapping unit. Chapter 3 provides dimensions,
environmental requirements, and interfaces that are useful to
design engineers wishing to interface to the Lisa.

Chapters 4 through 11 contain complete functional descriptions
and theory of operation for each module in the Lisa. These
chapters will not be of interest to the general reader; they
are intended for use only by design and service personnel.
Included is information on the:

    o Processor board
    o Memory board
    o I/O board
    o Video board
    o User interface
    o Floppy-disk drives
    o Power supply
    o Assembly.

Schematics for all modules are located in the appendixes.
Other relevant documents include the:

    o Lisa Owner's Guide
    o Operating System Reference Manual for the Lisa.
    o Profile Owner's Manual
    o Motorola 68000 User's Manual
    o Motorola 6504 User's Manual
    o Motorola 6522 Data Sheet
    o COPS421 User's Manual
    o 8530 SCC User's Manual
    o AMD 9512 Data Sheet.

CHAPTER 1. ARCHITECTURE
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The Lisa is a powerful, compact personal computer. It
features an integral screen, disk storage, and a large amount
of memory. In addition, you can add an extensive mix of input
and/or output (I/O) devices. Perhaps the most striking
hardware feature is the mouse, which the operator uses to
communicate with the Lisa software.

Details of the operation and use of the Lisa can be found
elsewhere; see the Preface for a list of related documents.
This manual provides an exhaustive description of the internal
workings of the Lisa for those who need to diagnose, repair,
or expand one.

1.1   Layout

The Lisa consists of a cabinet that houses the screen,
removeable hardware modules, and two floppy-disk drives,
and a detachable keyboard and mouse that plug into the
front and back of the cabinet, respectively.

Figure 1-1 presents a front view of the Lisa. Figure
1-2 shows the connectors and controls on the back of the
Lisa.

The hardware modules inside the cabinet are accessed by
removing the front and back panels. Note that removing
these panels causes the Lisa to turn off due to the
panel safety interlocks. Also note that this does not
remove power from the Lisa; to remove power, unplug the
line cord.

Chapter 3 describes the assembly of removeable hardware
modules in detail. Assembly and disassembly procedures
are available in other Lisa documents; see the Preface
for a list of related documents.

fats / pp.
add callouts

Chassis

FRONT

Screen

Dual Floppy
Disk Drives

ON/OFF
Switch

Keyboard Jack.

Keyboard.

Mouse

photo #
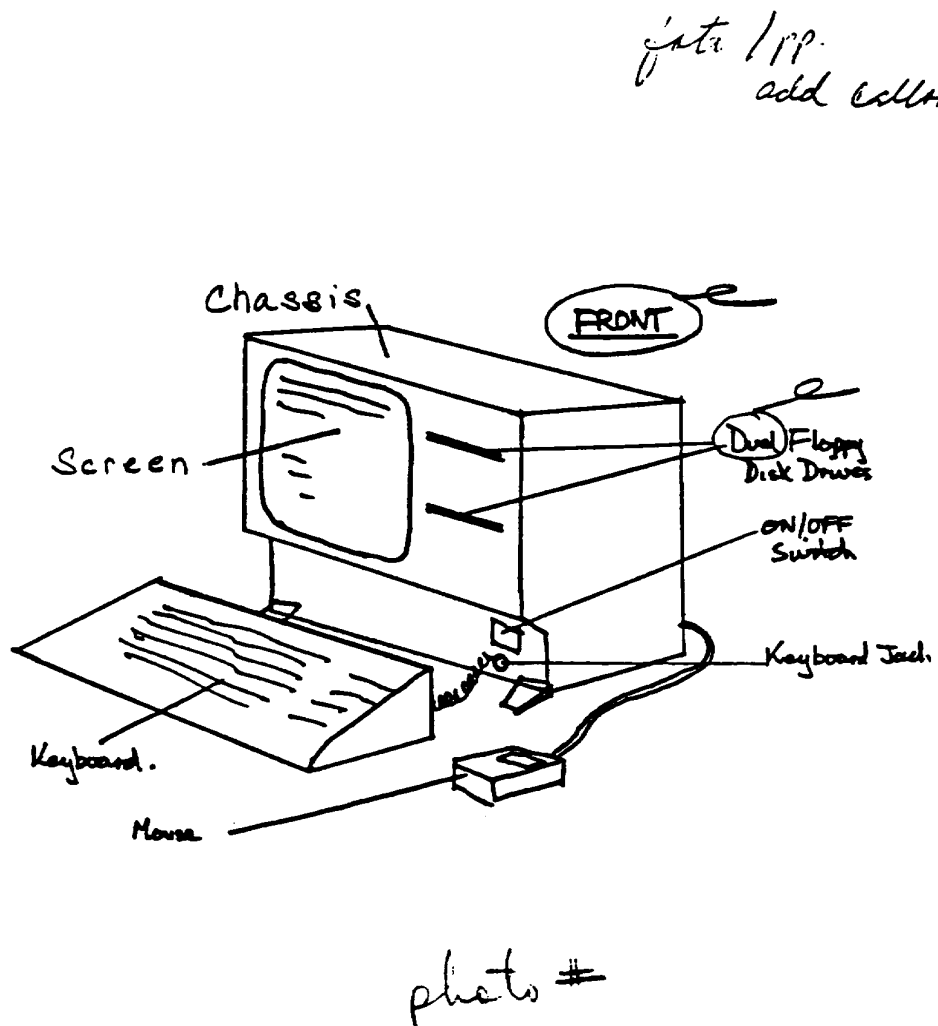
Figure 1-1. (System) Front View

1-2 A

September 7th 1982   LISA Hardware Manual
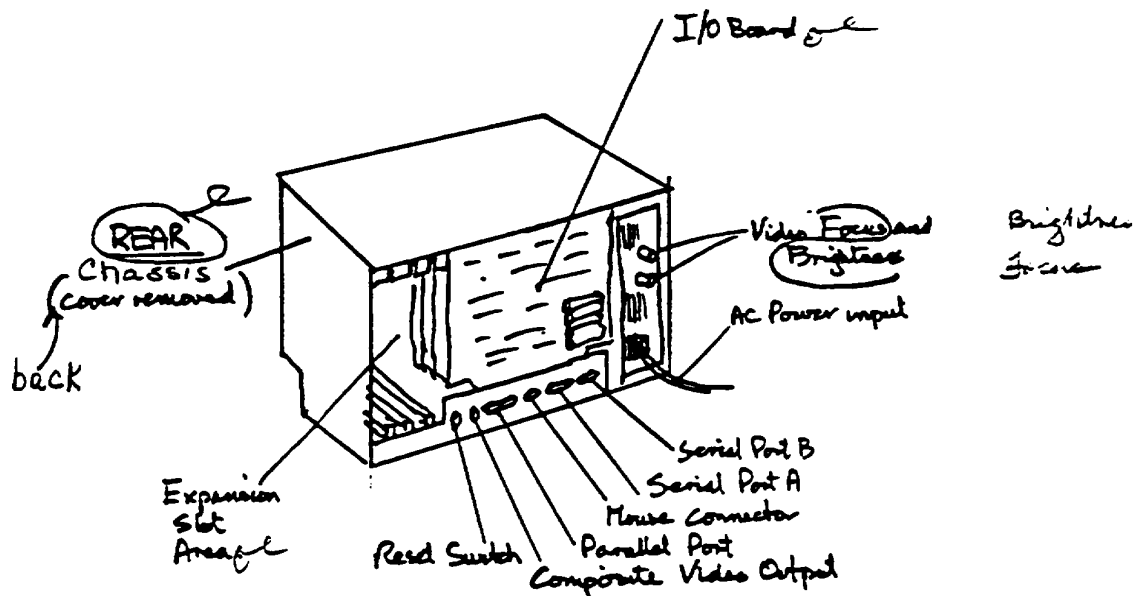
Figure 1-2. System Rear View with Panel Removed
Back

1-2B

1.2   Hardware Structure

The logic components of the Lisa are interconnected by
several buses, as shown in Figure 1-3. The main bus
connects the processor board with the I/O board and the
expansion slots.

Figure 1-3. Block Diagram

The heart of the Lisa is the processor board; it
contains the central processing unit (CPU), timing,
memory management unit (MMU), video generation logic,
I/O decode and interrupt logic. It also provides the
necessary control and timing signals for the memory
boards. The memory boards can be in several possible
configurations, depending on the size and type of memory
installed. The memory board contains the main random
access memory (RAM) matrix, plus parity generation and
checking, and some address decoding logic.

The Lisa communicates with the outside world principally
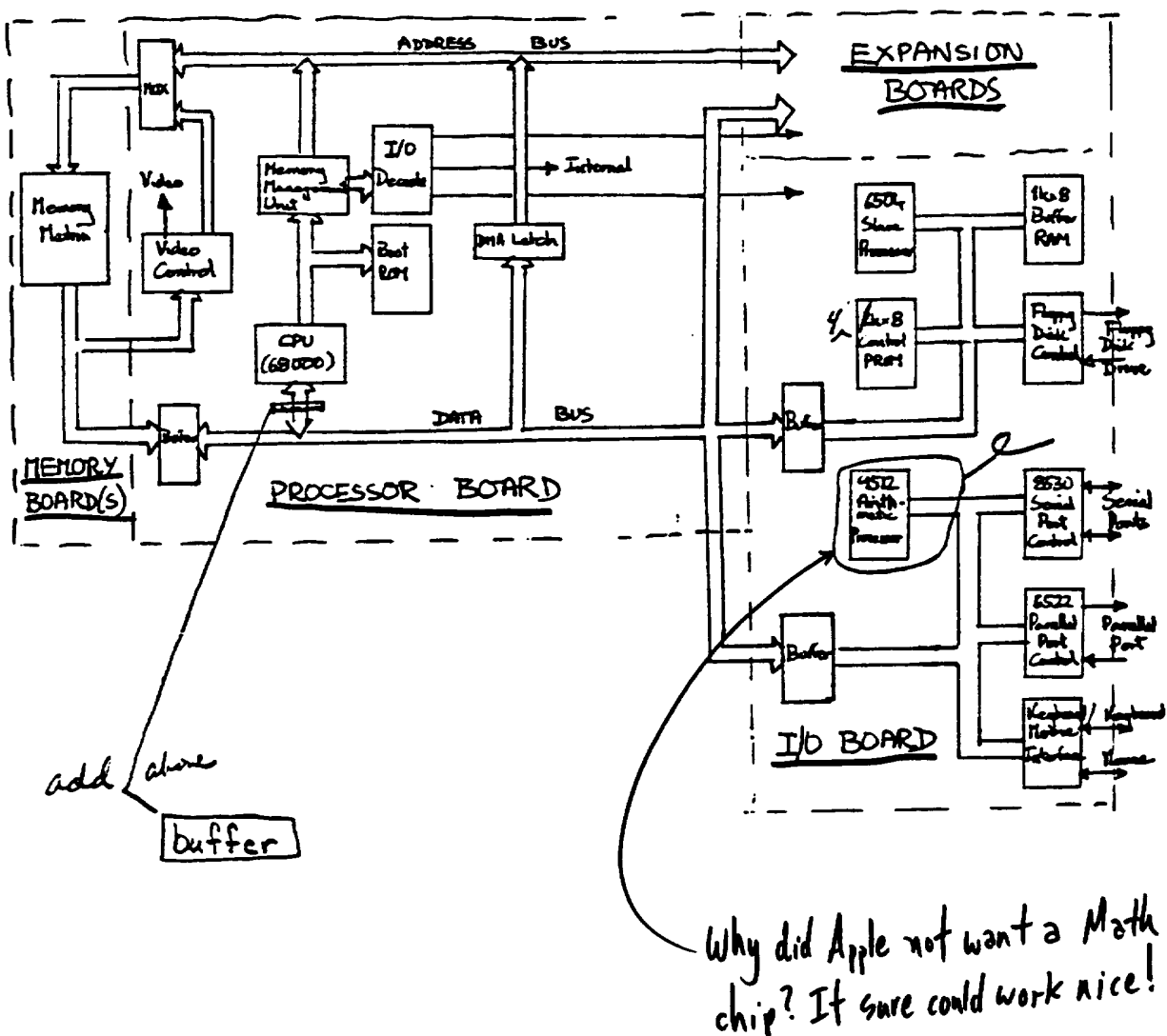
Figure 1-3.   ~~System~~ Block Diagram

1-48

through the I/O board. This board provides controllers
and interfaces for:

* Two serial I/O ports,
* A parallel port for peripherals, such as a hard
  disk or printer,
* Keyboard,
* Mouse,
* Speaker, and
* Floppy-disk drives.

Video contrast is also controlled by this board. In
addition, the CPU may have the use of an optional
arithmetic processing unit, located on the I/O board.

The video board is controlled both by the logic present
on the processor board and by the contrast latch on the
I/O board. It provides the analog logic necessary to
drive the video monitor. The video memory is used to
display an image organized as a bit map in main memory.

The expansion slots on the motherboard provide locations
for additional logic modules. A description of the bus
interface itself can be found in Chapter 3 of this
manual.

The disk drives accept standard Fileware diskettes. The
diskettes are described in a separate manual; see the
Preface for a list of related documents. An overview of
the disk drives is given in Chapter 9. Details of the
disk drives can be found in the relevant disk drive
manual; see the Preface.

The monitor is a high-resolution twelve-inch diagonal
monochrome cathode-ray tube (CRT) that uses a 60 hertz
(Hz) refresh rate. It displays individual pixels as
black or white only. There is no gray scale as such;
grays are displayed by intermixing black and white
pixels in the same area.

1.3   The Central Processing Unit

The Lisa's central processor is based on the Motorola
68000 processor chip. A block diagram of the 68000 is
shown in Figure 1-4. The 68000 provides:

* 32-bit data and address registers
* 16 megabyte (Mbyte) addressing range
* Memory-mapped I/O
* 14 addressing modes.

In addition to the seventeen 32-bit registers, a 32-bit
program counter, and a 16-bit status register, there
exists the possibility of configuring the general
purpose registers to allow for the width of the data
actually being used.

In the Lisa, the 68000 is driven by a 5 megahertz (MHz)
clock with a period of 200 nanoseconds (ns). The
processor memory access time is 800 ns. The CPU and the
video logic interleave memory accesses. Instruction
execution times must be a multiple of 800 ns. All
instructions that are longer than 800 ns have wait
states inserted if required, so that all instructions
execute in multiples of 800 ns.

Figure 4. Processor Block Diagram

1.4   Memory

The 68000 CPU generates 24-bit logical addresses to
access data in the Lisa. These are considered logical
addresses and the set of all possible addresses is the
16 Mbyte logical address space of the Lisa. The logical
address space is used to access all random access
memory, ROM or RAM, and I/O present in the Lisa.

In order to access one of these physical locations, each
logical address must be translated into a physical
address. A physical address can point to one of the
three possible physical address spaces in the Lisa.

September 7th 1982

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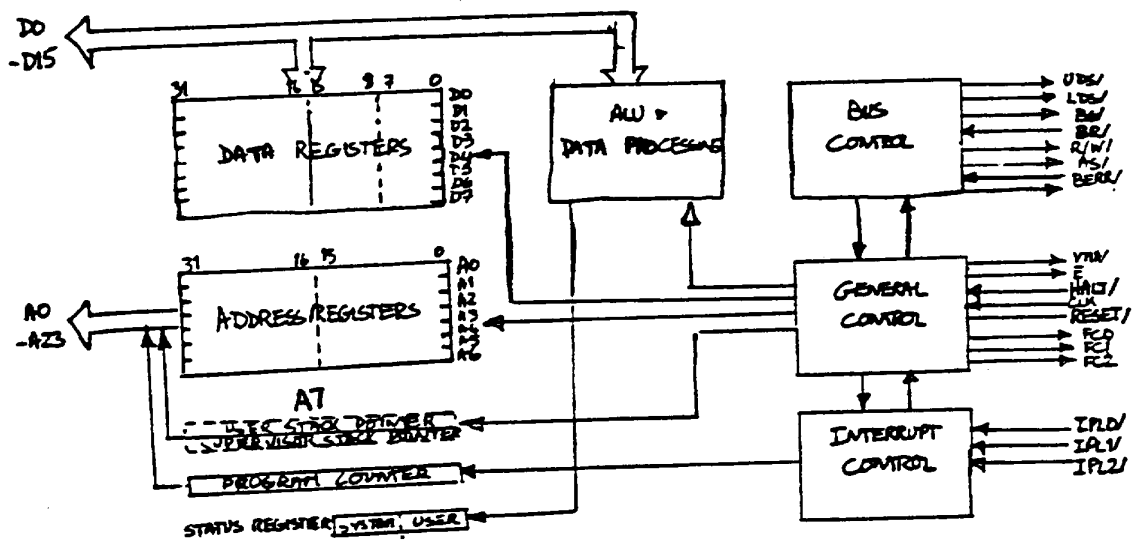
Figure 1-4. Processor Block Diagram

1-5b

These are:

* Main memory, 2 Mbytes of RAM,
* I/O space, I/O devices and latches,
* Special I/O, MMU registers and boot ROM.

The translation is performed by a method known as
relocation. It is implemented by a section of logic on
the processor board known as the MMU.

The main memory is where programs and data are stored
while in use by the Lisa. The MMU provides both the
translation of the address and flags that provide
further information on the type and accessibility of the
data. This is described in section 2.3

The I/O space is used to access peripheral controllers
and status and control registers. The special I/O space
is used to access bootstrap routines stored in
non-volatile ROM and also to access the registers
internal to the MMU where translation data is stored.
The MMU internal registers permit the operating system
to control the entire relocation process.

Within the MMU there are four identical sets of
translation registers, each representing a different
mapping of logical addresses into the three physical
address spaces. Each set is called a context.

Context 0 is reserved for use by the operating system,
while 1, 2 and 3 are available for the operator, who is
also referred to as the "user," programs. Only one
context is current at any given time. By switching
contexts, rapid switching between processes can be
affected under user control.

User programs only need to be aware which segments of
logical space are available to them and which of these
point to RAM and to valid I/O addresses. The MMU
performs access checks and classifies the type of
storage that they point to, such as stack memory, ROM,
and I/O space.

The maximum configuration of RAM storage that can be   ✓
present in the main memory is 2 Mbytes. Each physical
memory space within the Lisa is divided as shown in
Figure 1-5.

Special I/O space is not invoked during normal
operation. It is used during startup, and when the
registers that configure the MMU are being modified.
During normal operation, only the operating system has
access to special I/O space. Note that the operating

system is capable of providing this ability to any
program, although it would not be an advisable practice
to do so.

Since logical addresses make no distinction among the
three possible address spaces, each can be operated on
by the full 68ØØØ command set. Each physical address
space shown in Figure 1-5 is distinguished by signals
generated within the MMU. There is, therefore, no
physical overlap of memory space and no masking of any
memory area.

Hexadecimal Address Range	Physical Address Space	Function
ØØØØØØ-1FFFFF	Main Memory	RAM storage
ØØØØØØ-ØØ1FFF	I/O	Slot 1 low decode
ØØ2ØØØ-ØØ3FFF	I/O	Slot 1 high decode
ØØ4ØØØ-ØØ5FFF	I/O	Slot 2 low decode
ØØ6ØØØ-ØØ7FFF	I/O	Slot 2 high decode
ØØ8ØØØ-ØØ9FFF	I/O	Slot 3 low decode
ØØAØØØ-ØØBFFF	I/O	Slot 3 high decode
ØØCØØØ-ØØCFFF	I/O	FD Controller memory
ØØDØØØ-ØØDFFF	I/O	I/O board devices
ØØEØØØ-ØØEFFF	I/O	CPU board devices
xxØØØØ-xx3FFF	Special I/O	Boot & self-test ROM (16K)

Figure 1-5. Physical Memory Map

1.5   Internal Buses

The Lisa uses two bus structures to communicate between
hardware modules, such as the processor board, I/O
board, etc. Most boards communicate through the system
bus, which interconnects the processor board with the
I/O board and the expansion slots.

The system bus is based on the interface signals of the
68ØØØ CPU. Operations and timing on the bus follow
those of the 68ØØØ closely, although not identically.
Refer to Chapter 4 for a discussion of the system bus
and its operation.

The second bus, the memory bus, is a specialized set of
signals that are used by the processor board to provide
timing and control signals to the memory board(s).

1.6   Data Storage Media

The Lisa contains two high-density mini-floppy disk
drives. Disks from non-Lisa computers may not be freely
interchanged with those used in the Lisa, due to the
special encoding of disks format and media type.
Details of the disk drives can be found in Chapter 9 or
from the relevant disk drive manual; see the Preface for
a list of related documents.

In addition, a compatible hard-disk drive, such as
Apple's Profile, can be connected to the parallel port
to provide enhanced data storage capacity and access
time. Details of this interface can be found in Chapter
3. Format and storage capacity of this drive are a
function of the actual unit used. Details are beyond
the scope of this document.

1.7   User Interfaces

The user communicates with the Lisa by way of the
keyboard, as on a conventional computer, and by using
the mouse. In fact, most tasks can be completed without
typing.

You can roll the mouse around a small area beside the
Lisa to move a cursor around the CRT. Press the button
on top of the mouse to select among the available
functions displayed on the CRT.

1.8   Additional Features

A real-time clock has been incorporated into the I/O
board. The clock keeps the correct time, and is
available to the programmer for use in a number of
applications where measurement of elapsed time or the
current date and time is important.

The Lisa is also equipped with a battery-backup unit.
This enables the real-time-clock to function while the
Lisa is entirely disconnected from a power source. It
also preserves the contents of the parameter memory.

CHAPTER 2. PROGRAMMING
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This chapter describes the interface that the Lisa hardware
provides to the software. It is not intended as an exhaustive
description of the operating system, nor should it be regarded
as a specification of required parameters for an operating
system on the Lisa. Refer to the Preface for the names of
manuals that contain programming details.

2.1   The Instruction Set

The instruction set of the Lisa is essentially that of
the 68000 processor. Differences occur only in the
details of addressing the memory and I/O in the Lisa.
Instructions can be categorized into four possible modes
of logical addressing:

* Data: When an effective address mode refers to
  data operands, it is considered as a data
  address mode.

* Memory: When an effective address mode refers
  to memory operands, it is considered a memory
  address mode.

* Alterable: When an effective address mode is
  used to refer to writeable operands, it is
  considered an alterable address mode.

* Control: When an effective address is used to
  refer to memory operands without an associated
  size, it is considered a control address mode.

It is possible to combine these categories within the
instruction set, resulting in more specialized
categories. For example, data alterable refers to
address modes that are both data and alterable.

Note that the status register addressing mode is not
permitted unless it is explicitly mentioned as a legal
addressing mode.

The full instruction set is not discussed here. Details

are available in the 68ØØØ User's Manual.

2.2   CPU Registers and Their Use

There is a 16-bit status register, which consists of a
user byte and a system byte. In addition, there are a
number of 32-bit registers in the CPU that are available
to the user. These are:

   * 8 Data registers
   * 7 Address registers
   * 1 User stack pointer
   * 1 Supervisor stack pointer
   * 1 Program counter.

The status register contains a number of coded bits,
divided into a user byte and a supervisor byte. The
supervisor byte contains the trace and supervisor flags,
plus a three-bit code showing the current interrupt
mask. The user byte contains the condition codes.
Refer to the 68ØØØ user manual for a full discussion.

The data registers can be used for bit, byte, word, or
long-word operations. The address registers can be used
as word or long-word registers. Both the address
registers and the stack pointer can be used as software
stack pointers and base-address registers. All data,
address, and stack pointer registers can be used as
index registers.

Where a data register is used to store less than the
full 32-bit capacity, the bit, byte, or word is stored
in the low-order part of the register. The least
significant bit (LSB) is bit zero and the most
significant bit (MSB) is bit 31.

Address registers provide either the low-order word, or
the full 32-bit long word, as the source operand,
depending on the operation. When used as a destination,
the entire register is affected, regardless of the size
of the operand required in the operation.

2.3   Memory Management Scheme

The MMU is a hardware device that translates logical
addresses emitted by the CPU into physical addresses for
objects in main memory or I/O space. At the same time,
it provides access controls that are preset by the
operating system. These prevent a particular program
from accessing areas of memory outside of the portion
assigned to it.

Figure 2-1. Address Word Decode

2-3b
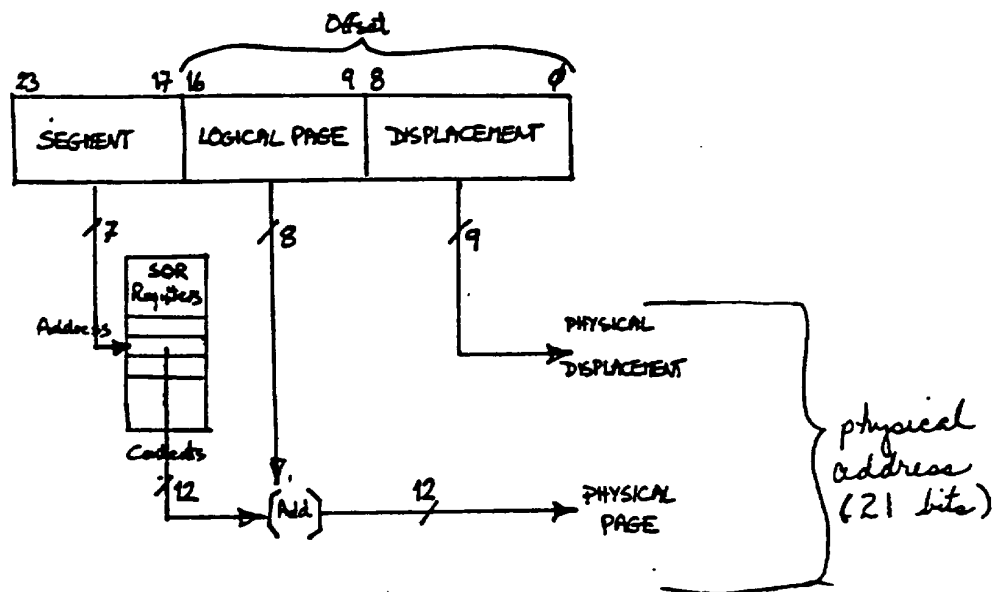
The logical address provided by the CPU consists of 24
bits. These are interpreted by the MMU in three
sections. The first section consists of bits 23 through
17 and is the logical segment number. The second
section consists of bits 16 through 9 and provides the
logical page displacement. The third section consists
of bits 8 through 0 and gives the displacement, both
logical and physical, within the page. This can be seen
in Figure 2-1.

Figure 2-1. Address Word Decode

Logical addresses can point to any part of the 16 Mbyte
addressing space. The MMU interprets these logical
addresses on the basis of parameters loaded into its
registers by the operating system.

The Lisa's memory physically occupies 2 Mbytes of
physical address space. This would imply that only 16
segments, each of 128 kilobytes (Kbytes) can be used
meaningfully. However, each segment's physical address
space does not necessarily occupy the full 128 Kbytes
allotted to it in logical address space. Each segment
can be mapped into as little as one 512-byte page of
physical memory. Therefore many more than 16 logical
segments can map into the 2 Mbyte memory space.

Each segment within the MMU has two registers associated

with it. The first is known as the Segment Origin
Register (SOR). It describes the physical origin of the
segment, which is a page boundary within the memory.
The second is the Segment Limit Register (SLR). It
describes both the size in terms of 512-byte pages and
the type of space being addressed.

Each context in the MMU consists of a table of 128
segment descriptars consisting of the SOR and SLR. The
segment number, bits 23-17 of the logical address, is
used to index into the table and retrieve the value
stored in the SOR and SLR.

2.3.1 Address Transformation

Logical address space is divided into 128 logical
segments. Each segment consists of up to 256 pages
of 512 bytes per page. Therefore, the maximum
segment size is 128 Kbytes and the minimum is 512
bytes.

The SOR register contains the 12-bit page address in
physical space where the corresponding physical
segment begins. The entire segment is located in
physical space with respect to this origin. The
logical page displacement given by the second
section of the logical address, bits 16-9, is added
to the contents of SOR to produce the physical page
address being accessed. The logical operation is
shown in Figure 2-1. The least significant nine
bits of the logical address translate directly into
the physical displacement.

The SLR contains the size limit of the physical
segment, given as a number of pages, plus control
bits that define the type of the segment. This
indicates which of the three physical address spaces
the segment is contained in: memory, I/O, or
special I/O. It can also indicate the memory use,
such as read-only or stack.

Once the SOR contents and logical page displacement
have been added, the MMU performs a limit check to
see whether the resulting physical page lies within
the limits given by the SLR. The logical operation
performed is shown in Figure 2-2.

The SLR contains control and limit data. The four
high-order bits of the register contain control
information. The eight low-order bits contain the
number of pages in the segment, which is compared
with the page offset in the logical address.

If the address is within the physical segment, the
access proceeds. If the address lies outside the
segment, the access is terminated and an error
condition is presented to the CPU.

The physical address word consists of 21 bits.
These 21 bits are sufficient to address a space of 2
Mbytes.

Figure 2-2. Segment Limit Check

2.3.2 The MMU Registers

The MMU registers are physically a matrix of 1024
12-bit registers. These are divided into four sets
of 128 pairs of registers, one for each of the four
contexts in which the Lisa may operate. The
technique of switching contexts is used to
reconfigure the Lisa rapidly when switching between
processes.

All MMU registers are addressed in special I/O
space; refer to Figure 1-5. The contents of the SOR
are modified or read by accessing an address in
special I/O space, as shown in Figure 2-3.
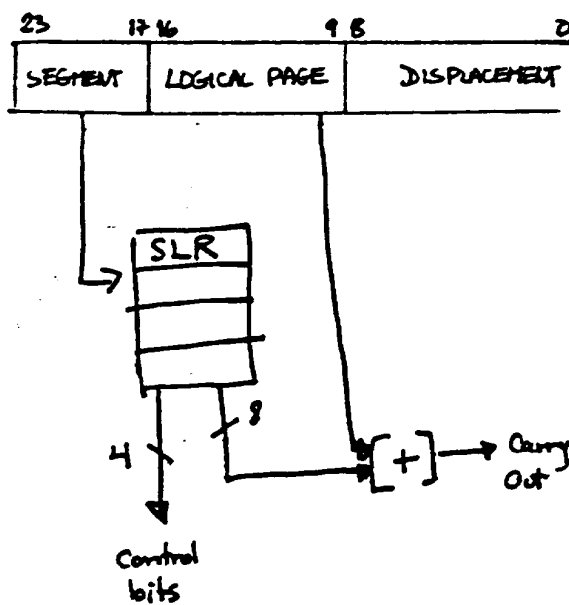
Figure 2-2. Segment Limit Check

2-5b
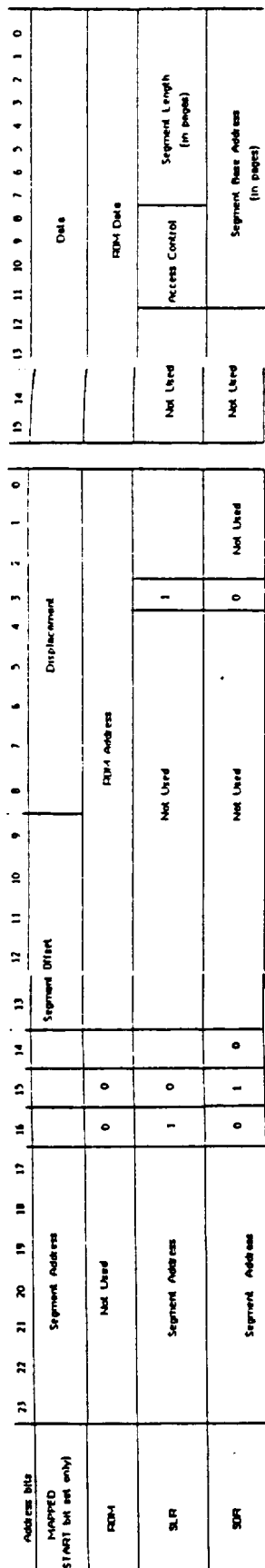
Figure 2-3. Special I/O Addressing

A segment which was to begin at the physical address

2-6   31 May 1983 @9am

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000200@16 would have its corresponding SOR set to
0001@16. The SOR contains the origin in terms of
multiples of 512-byte pages in the physical space.

The segment length is interpreted by the 68000 IN
TWO'S COMPLEMENT FORM. Care should therefore be
taken in loading the limit to be used. A length of
00 implies a segment of maximum length, 128 Kbytes.
A length of FF@16 implies the minimal segment length
of 512 bytes, one page.

An exception to the above occurs in the case of a
stack segment, which is flagged as such by the
control bits. In the case of a stack, usage of the
segment begins at the top of the segment and
decrements. Thus 00@16 implies one page, 512 bytes,
and FF@16 implies 128 Kbytes for a stack segment
only.

The access control bits are used to restrict program
manipulation of the data pointed to in the area of
memory. The bit significance is shown in Figure
2-4.

To set up the MMU registers, the SOR and SLR
registers must be set up by the operating system for
each of the 128 possible segments.


```
     Bit
11 10  9  8      Address space and access limitation
_____
 0  1  0  0      Main memory -- read only from stack
 0  1  0  1      Main memory -- read only
 0  1  1  0      Main memory -- read/write to stack
 0  1  1  1      Main memory -- read/write
 1  0  0  1      I/O space
 1  1  0  0      Page invalid (segment not present)
 1  1  1  1      Special I/O space
 0  0  0  0      )
 0  0  0  1      )
 0  0  1  0      )    Invalid Codes
 1  0  0  0      )
 1  0  1  0      )  (Unpredictable results
 1  0  1  1      )        will occur)
 1  1  0  1      )
 1  1  1  0      )
```

Figure 2-4. MMU Access Control Bits

2.3.3 MMU Initialization

When the Lisa performs a Power-On Reset (POR), the
MMU registers are in an unknown state. In order to
write to the MMU registers, the START bit must be
set. This is satisfied automatically at power-on
time, or by the software accessing I/O address
$00E010@16$.

When the START bit is set, bit 14 of the address
acts as a switch between special I/O space and other
address spaces. During initialization, bit 14 must
be 0 to execute from ROM in special I/O space. A
$1111@2$ code output for the access bits of the SLR
registers is provided by hardware in setup mode.
The MMU is not needed to address the boot ROM, so
the boot program does not require the MMU to be
initialized.

The boot ROM initializes the MMU so that physical
memory is contiguous and starts at address 0.
Accesses higher than the top of physical memory are
not allowed except for segment 126 (addresses of the
form FCxxxx@16) addresses I/O space, and segment 127
(addresses of the form FExxxx@16) addresses special
I/O.

To set the MMU registers, the MMU is disabled. This
is done by setting the START bit. This bit is set
automatically at power-up when the MMU registers are
uninitialized. It must be set whenever the MMU
registers are being loaded.

In order that a program in RAM may continue to
execute when the START bit is set, a hardware switch
is incorporated which permits execution via the
MMU. This avoids the need to invoke a subroutine in
ROM, which would otherwise be necessary. Address
bit 14 controls the switch and the program executing
in RAM must execute with address bit 14 set 1.

RAM continues to be accessible via the MMU whenever
address bit 14 is high while the START bit is set.
Thus, any access to a location whose address has bit
14 set results in the MMU performing an address
translation, just as in normal processing. By using
this feature, it is possible to access both normal
mapped address space, and non-mapped special I/O
space under control of program addressing.

A program that alters any of the MMU register
contents is typically run only in supervisor mode.

2.3.4 Contexts

To permit fast switching among program environments,
the MMU provides four contexts in which programs can
run. The context in which the Lisa is currently
running is selected by two control bits, SEG1 and
SEG2. The operating system typically runs in
context 0. User programs execute in one of the
other three contexts. When transfer of control to
the Lisa and back is required, such as might happen
for interrupt handling, the SEG bits are configured
to select the new context. Since the MMU has
completely independent sets of SOR and SLR registers
for each context, context maps are independent of
each other.

These bits are located on the processor board and
modified as described in subsection 2.5.5. Context
is selected by configuring the SEG1 and SEG2 bits to
give the required context as shown below:

SEG2	SEG1	Context
0	0	0
0	1	1
1	0	2
1	1	3

Context 0 is intended for exclusive use of the
operating system, while contexts 1, 2, and 3 are
intended for general purpose use. The Lisa
automatically selects context 0 whenever an access
is made in supervisor mode. Thus a TRAP instruction
can be used to generate a call from a user process
to the operating system.

Normally, the context is changed while executing in
supervisor mode. Execution in the new context
begins when user mode is entered.

The context is loaded by a read or write to certain
addresses in I/O space, as follows:

        00E00A@16   set SEG1
        00E008@16   reset SEG1

        00E00E@16   set SEG2
        00E00C@16   reset SEG2

2.4   Addressing in Special I/O Space

In special I/O space, it is misleading to talk in terms
of address translation as used in normal memory space.
The address in special I/O space has several meanings,
depending on the state of bits 14 and 15.

The address is divided into a number of fields. Either
the segment number used to address an MMU register will
be present in bits 17 thru 23 or a ROM address will be
present in bits 1 thru 13, but not both.

The exact significance of the bits is shown in Figure
2-3 above. The format of a word used to alter an MMU
register is:

        SSSSSSS$\emptyset$1$\emptyset$xxxxxxxxxxxBxxx

The "S" designates the bits that select the segment for
which the registers are to be altered. The "x"
indicates a "don't care" condition. The "B" is a 1 to
write to the SOR and a $\emptyset$ to write to the SLR.

When the ROM is to be addressed, the word has the
format:

        xxxxxxx$\emptyset\emptyset\emptyset$RRRRRRRRRRRRRRR (START bit set)
    OR
        SSSSSSS$\emptyset\emptyset\emptyset$RRRRRRRRRRRRRRR (via the MMU)

Each "x" bit is ignored. The "S" bits are the address
of the segment that points to special I/O space. The
"R" bits are used as an address for the boot ROM
directly. That is, they are not translated by the MMU.

A program that alters any of the MMU registers should
only be run in supervisor mode.

2.5   I/O Map

As outlined in Chapter 1, the Lisa contains
memory-mapped I/O and a special I/O space. The special
I/O space is invoked at power-up time and during
accesses to the MMU registers.

A full list of the I/O addresses within the Lisa is
given here, along with the bit significance of the data
written to and read from each address. An overview of
the full I/O space map is given in Figure 2-5. Note
that the best ROM assigns segment 126 to the 11$\emptyset$ space,
so all accesses to I/O space using the default MMU setup

have a logical address of FCxxxx@16.

```
        Address                 Function
        (hexadecimal)
        ----------------------------------------------------------
        FC      FC
        000000-001FFF           Expansion slot #1 Low Decode
        002000-003FFF             "       "   "  High Decode
        004000-005FFF           Expansion slot #2 Low Decode
        006000-007FFF             "       "   "  High Decode
        008000-009FFF           Expansion slot #3 Low Decode
        00A000-00BFFF             "       "   "  High Decode
        00C001-00C7FF           Floppy Disk Control   (see 2.5.1)
        00D000-00D3FF           Serial Ports Control (see 2.5.2)
        00D800-00DBFF           Parallel Port Control (see 2.5.3)
        00DC00-00DFFF           Keyboard/Mouse Control (see 2.5.4)
        00E000-00E01E           CPU board Control     (see 2.5.5)
        00E01F-00E7FF           (not used)
        00E8xx                  Video Address Latch
        00F0xx                  Memory Error Address Latch
        00F8xx                  Status Register
```

$FCxxxx

Figure 2-5. I/O Space Overview

2.5.1 Floppy Disk Control

The floppy-disk controller is located on the I/O
board and is controlled by addressing the portion of
physical I/O space in the range
00C001@16-00C7FF@16. This area contains command and
status data as described below.

The floppy-disk controller consists of a 6504 based
microcomputer, which has 4 Kbytes of program ROM for
its own exclusive use and 1 Kbyte of buffer RAM that
is shared with the main CPU. This RAM is provided
with power backup by a battery. Parameters stored
in the floppy-disk controller RAM are therefore not
lost during power down.

The low 16 words of the 6504 address space are
treated as a command block. The first byte is used
for communication between the CPU and the 6504. The
others are used to pass parameters for use in
defining command data and status.

Controller commands are written to 00C001@16 and
have the significance shown in Figure 2-6.

```
Code            Operation
-----------------------------------------------------------------
81@16           Execute the RWTS routine (parameters are given
                       by FCC∅∅3-FCC∅∅F@16)
82@16           Not used
83@16           Seek to side/track
84@16           JSR to routine pointed to by ∅∅C∅∅3-5
85@16           Clear Interrupt Status
86@16           Set Interrupt Mask
87@16           Clear Interrupt Mask
88@16           Wait in ROM until called to do cold start
89@16           Loop in ROM
```

Figure 2-6. Floppy-Disk Commands

The main part of the 65∅4 code consists of a
Read/Write/Track/Sector (RWTS) routine. This
utilizes a command block in the 8 bytes of memory
that should be configured by the CPU in accordance
with Figure 2-7.

```
Address            Operation
--------------------------------------------------------
FCC0003@16         Command Code
                   00@16 Read
                   01@16 Write
                   02@16 Unclamp
                   03@16 Format
                   04@16 Verify
                   05@16 Format Track
                   06@16 Verify Track
                   07@16 Read (without checksum verify)
                   08@16 Write (without checksum )

FCC0005@16         Drive Select
                   00@16 Drive 2 (lower)
                   80@16 Drive 1 (upper)

FCC0007@16         Side Select
                   0x@16 Side 1 (upper)
                   1x@16 Side 2 (lower)

FCC0009@16         Sector Number (0 to 22)

FCC000B@16         Track Number  (0 to 44)

FCC000D@16         Speed Byte

FCC000F@16         Format Confirmation Byte

FCC011@16          Error Status

FCC013@16          Disk ID Value
```

Figure 2-7. Floppy-Disk Command Block

The disk drives generate an interrupt to the CPU
whenever a diskette is inserted or a diskette eject
button is pressed. An interrupt is also generated
upon completion of an "81@16" command. The status
of the controller can be found by examining location
00C05F@16, as shown in Figure 2-8

```
            ERROR CODES          SIGNIFICANCE
         ------------------------------------------------------
                 Ø1 (hex)        Invalid Command
                 Ø2              Invalid Drive
                 Ø3              Invalid Sector
                 Ø4              Invalid Side
                 Ø5              Invalid Track
                 Ø6              Invalid Clear Mask
                 Ø7              No Disk
                 Ø8              Drive Not Enabled
                 Ø9              Interrupts Pending
                 ØA              Invalid Format Confirmation
                 ØB              ROM Selftest Failure
                 ØC              Unexpected IRQ or NMI

                 14              Write Protect Error
                 15              Unable to Verify
                 16              Unable to Clamp
                 17              Unable to Read
                 18              Unable to Write
                 19              Unable to Unclamp
                 1A              Unable to Find Calibration
                 1B              Unable to Adjust Speed
                 1C              Unable to Write Calibration
```

Figure 2.8. Floppy-Disk Controller Error Codes

Note that the interrupt flag must first be enabled
or a bus error will occur. The enable bit must be
high in order to be able to access the floppy RAM
that is shared by the floppy-disk controller and the
processor board. The interrupt source is identified
by this status byte, the bit interpretation being
coded according to Figure 2-9.

The disk controller has an area of memory that can
be used for CPU storage of parameters. It is
located between ØØC181@16 and ØØC1FF@16.

The memory area used for information transfer to and
from the disk controller is shared by the CPU and
the 65Ø4 and is located between ØØC5Ø1@16 and
ØØC7FF@16.

Bit	Significance
7	Set if bits 4, 5 or 6 set
6	Set if RWTS complete for Drive 2
5	Set when button on Drive 2 is pushed
4	Set when disk in place on Drive 2
3	Set if bits 0, 1 or 2 set
2	Set if RWTS complete for Drive 1
1	Set when button on drive 1 is pushed
0	Set when disk in place on Drive 1

Figure 2-9. Floppy-Disk Interrupt Source

2.5.2 Serial Port Control

The serial logic interface is implemented by a
serial communication controller (SCC) dual channel
device. Refer to the 8530 serial communication
controller manual for details.

The two serial interfaces in the Lisa are accessed
via the peripheral control device by accessing four
distinct addresses in I/O space, as shown below.

Channel A	Data:	00D247@16
	Control:	00D243@16
Channel B	Data:	00D245@16
	Control:	00D241@16

The baud rate for each of the two channels is
defined in terms of two time constants, which must
be loaded into the SCC. The time constants are
governed by the formulas:

$$TC(A) = 4,000,000/(2 \times Baudrate) - 2$$

$$TC(B) = 3,686,400/(2 \times Baudrate) - 2$$

This results in a table of baud rate values shown in
Figure 2-10. The serial ports use autovectoring,
which eliminates the need for the SCC to supply
interrupt vectors to indicate the source of the
interrupt to the CPU.

Baud Rate	Clock Multiplier	TC(A)	Error (%)	TC(B)	Error (%)
19200	16	—	--	4	0
9600	16	11	-0.16	10	0
4800	16	24	-0.16	22	0
2400	16	50	-0.16	46	0
1200	16	102	-0.16	94	0
300	16	414	-0.16	382	0
110	16	1134	-0.03	1045	0
19200	1	102	-0.16	94	0
9600	1	206	-0.16	190	0
4800	1	414	-0,16	382	0
2400	1	831	-0.04	766	0
1200	1	1664	-0.04	1534	0
300	1	6664	-0.01	6142	0
224000(Applebus)	1	—	--	6	0

Figure 2-10. Serial Port Baud Rates

2.5.3 Parallel Port Control

> The parallel port is controlled by a 6522 versatile
> interface adapter (VIA). There is a direct
> correspondance between the hardware lines on the
> physical connector and the assigned line within the
> 6522's two-byte ports. Refer to subsection 3.5.2
> for a discussion of the signal lines on the
> interface. The relationship between the 6522 port
> bits and the interface signals is shown in Figure
> 2-11.

6522 Controller line		Parallel Port line		Pin
PA∅–PA7	Peripheral A port	DD∅–DD7	Data Lines	
CA2	Control Line 2 A	PSTRB/	Processor Strobe	15
CA1	Control Line 1 A	BSY	Busy	16
PB∅	Periph. B Port ∅	OCD	Open Cable Detect	19
PB1	Periph. B Port 1	BSY	Busy	16
PB2	Periph. B Port 2	DEN	Disk Enable	–
PB3	Periph. B Port 3	DRW	Read/Write	3
PB4	Periph. B Port 4	CMD/	Command	17
PB5	Periph. B Port 5	DIAGPAR	Diagnostic Parity	–
CB2	Control Line 2 B	PARITY/	Interface Parity	18
(PB5)	Keyboard B Port 5	PRES/	Parity Reset	–
(PB7)	Keyboard B Port 7	CRES/	Controller Reset	21
	See note	CHK	Check	25

      Notes: The last three signals are connected to the
              keyboard 6522.

              The BSY signal connects to both the CA1
              and PB1 lines.

              The check line is encoded by the keyboard
              interface and produces an independent
              interrupt and key code D∅∅∅@2 ∅1∅1@2,
              where D is a 1 on a rising edge and a ∅
              on a falling edge.

Figure 2-11. Parallel Port Bit Correspondance

        Note that some bits on this 6522 are used for
        signals other than those for the parallel port.
        Also note that two bits for the parallel port are
        controlled via the keyboard 6522. The programming
        of the 6522 is described in the 6522 data sheet.
        The addressing scheme is given in Figure 2-12.

```
Address    Register #  Function
(hexidecimal)
```

Address (hexidecimal)	Register #	Function
00D901	0	ORB/IRB (Input/Output Register)
00D909	1	ORA/IRA (Input/Output Register)
00D911	2	DDRB (Data Direction Register)
00D919	3	DDRA (Data Direction Register)
00D921	4	T1C-L (Low-order Latch/Counter)
00D929	5	T1C-H (High-order Counter)
00D931	6	T1C-L (Low-order Latches)
00D939	7	T1C-H (High-order Latches)
00D941	8	T2C-L (Low-order Latch/Counter)
00D949	9	T2C-H (High-order Counter)
00D951	10	SR (Shift Register)
00D959	11	ACR (Auxiliary Control Register)
00D961	12	PCR (Peripheral Control Register)
00D969	13	IFR (Interrupt Flag Register)
00D971	14	IER (Interrupt Enable Register)
00D979	15	ORA/IRA (as for 1 w/o handshake)

Figure 2-12. Parallel Port Addressing

If CA1 is in pulse handshake mode and the DEN bit is
low, the CA1 line pulses to transfer data to or from
the parallel port each time that data is read from
or written to the A port. CA1 is fed directly to
CA2 to allow latch mode to be used on the A port
while data is being read.

The CR/ signal is generated by manipulation of the B
port on the keyboard interface. Refer to subsection
2.5.4 for details.

2.5.4 Keyboard/Mouse Control

Keyboard and mouse control are performed by a
dedicated slave processor, known as a
control-oriented processor system (COPS). It
provides communication with four peripheral devices
via the A port of the keyboard 6522 VIA port
controller. These devices are the:

* Keyboard
* Mouse
* Real-time clock
* Software power-off.

Commands to these peripherals are written to the A
port of the 6522 and data is fetched from the same
location. The keyboard and mouse are addressed
using the 6522 registers as shown in Figure 2-13.

Address (hexidecimal)	6522 Register #	Function
00DD81	0	ORB/IRB
00DD83	1	ORA/IRA
00DD85	2	DDRB
00DD87	3	DDRA
00DD89	4	T1C-L
00DD8B	5	T1C-H
00DD8D	6	T1C-L
00DD8F	7	T1C-H
00DD91	8	T2C-L
00DD93	9	T2C-H
00DD95	10	SR
00DD97	11	ACR
00DD99	12	PCR
00DD9B	13	IFR
00DD9D	14	IER
00DD9F	15	ORA/IRA (Same as in register 1, but without handshake)

Refer to 6522 Data Sheet for details

Figure 2-13. Keyboard/Mouse Addressing

The abbreviations used in Figure 2-13 refer to
registers within the 6522, similar to Figure 2-12.
The 6522 is described in the 6522 data sheet.

The command format to the COPS is shown in Figure
2-14.

```
Keyboard
6522 PA Port    Function
7654 321Ø
--------------------------------------------------------------------
ØØØØ ØØØØ        Turn I/O port on
ØØØØ ØØØ1        Turn I/O port off
ØØØØ ØØ1Ø        Read Clock Data
ØØØ1 nnnn        Write nnnn to clock
ØØ1Ø spmm        Set Clock Modes, where:
                     s=enable (1) or disable (Ø) clock set mode
                     p=power on (1) or off (Ø)
                     mm = ØØ  Clock/Timer Disable
                          Ø1  Timer Disable
                          1Ø  Timer Underflow Interrupt
                          11  Timer Underflow Power-On
Ø1Ø1 nnnn        Set NMI character high nibble to nnnn
Ø11Ø nnnn        Set NMI character low nibble to nnnn
1xxx xxxx        No operation
```

Figure 2-14. Keyboard COPS Commands

Note that, in addition to the keyboard and mouse,
several other peripherals are interfaced to the Lisa
via the keyboard 6522. These are:

  * Two parallel-port lines
  * Three volume-control lines
  * Speaker tone line
  * Floppy-disk interrupt.

The COPS receives power from the backup supply.
This voltage is available at all times, whether the
Lisa is powered down or even unplugged. The only
time the COPS ceases functioning is if the battery
is allowed to run down by having the Lisa unplugged
over a long period.

This means that the COPS is always operational. It
keeps the time of day and provides software control
of the power on and off functions.

Keyboard

    The keyboard on the Lisa is a true N-key rollover
    design. An arbitrary number of keys can be
    depressed without causing phantom key problems.
    The key codes returned by the interface are in the
    form:

                         drrr@2 nnnn@2

          where "d" indicates direction of keystroke
          (down=1, up=0), and "rrr" and "nnnn" are given in
          Figure 2-15.

                    Figure 2-15. Lisa Keyboard Codes

Fig. 2-15 : Keyboard Codes
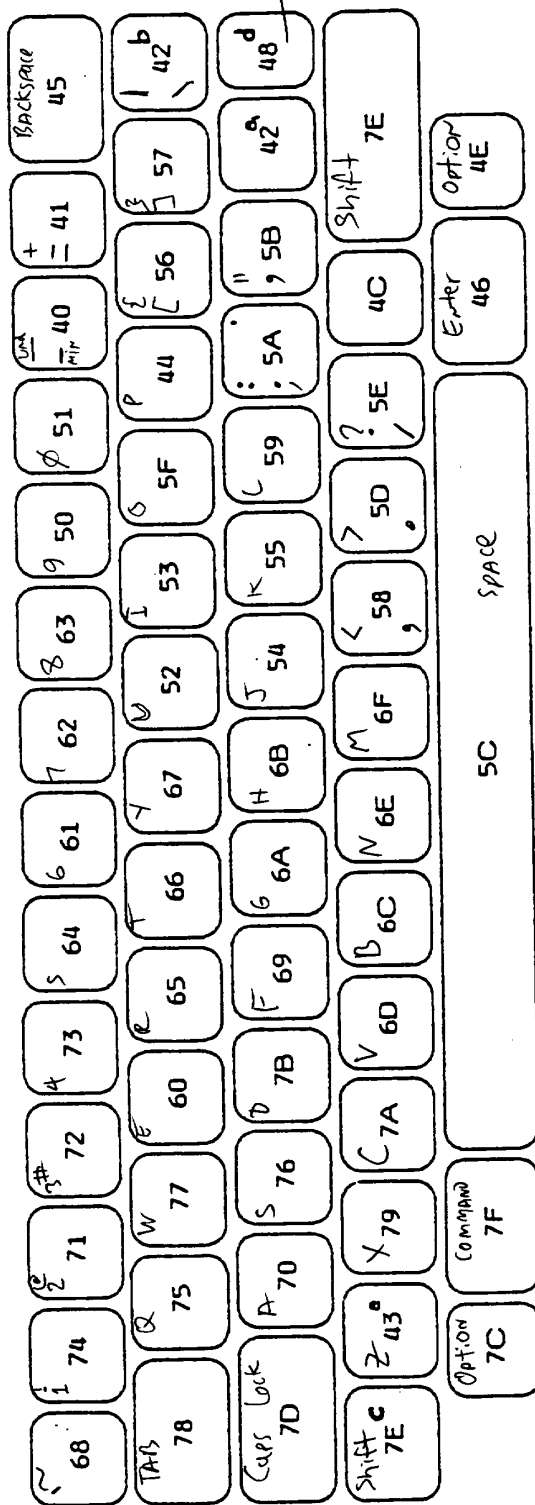
Keycodes

All keycodes are in hexadecimal, with the following format in binary:

drrr nnnn

d=0, upcode
d=1, downcode
rrrnnnn=above keynumber

l.c.?

Notes:

a. Not on US layout

b. Not on European layout

c. Key 7E is shaped to fill the hole of the unused keys 43 on US layout.

d. Key 48 is shaped to fill the hole of the unused key 42.
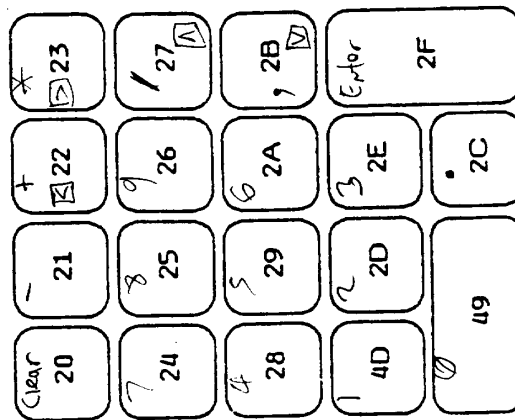
Software must interpret such functions as shift
and auto-repeat. Any key can be programmed to
generate a non-maskable interrupt.

In addition to key information, a number of
two-byte sequences that are known as reset codes
are produced. Each sequence consists of a reset
character, 8Ø@16, followed by a code number. The
significance of the code numbers is shown in
Figure 2-16.

Reset Code (hexadecimal)	Significance
FF	Keyboard COPS failure detected
FE	I/O Board COPS failure detected
FD	Keyboard unplugged. The reset code of the keyboard identification follows when the keyboard is plugged back in.
FC	Clock timer interrupt
FB	"Soft power off" switch has been depressed
FA) .) .) .) F0)	Reserved for future use
Ey	Clock data follows. Five bytes are transferred after this. "y" is the year, coded in the reset byte. The other bytes have the format: (80 Ey) dd dh hm ms st where ddd is the day, hh the hour, mm the minute, ss the second and t the tenths of a second.
DF) .) .) .) 00)	Keyboard ID number. This code is produced whenever the keyboard COPS is reset. At present, the valid codes are:

Single nibble allows
a 16 year span:
0 to 15
$0 to $F

	HEX		LAYOUT
KEYTRONICS		APD	
$AD		$2D	French
$AE		$2E	German
$AF		$2F	UK
$BF		$2F	US

Figure 2-16. Keyboard COPS Reset Codes

Mouse

The mouse connects to the COPS. Mouse commands
have the format:

Ø111@2 ennn@2

If "e" is set, mouse interrupts are enabled. The
"n" bits define the time interval that separate,
mouse interrupts. The time interval is the binary
value of "nnn" times 4 milliseconds. Whenever you
move the mouse, it interrupts the processor with
this period.

Mouse data are transferred to the CPU in three
bytes. These are polled from the keyboard 6522 A
port. The significance of the bytes is as
follows:

ØØ	Mouse data follows
dx	Change in x direction (-127 to 127)
dy	Change in y direction (-127 to 127)

Each time the value is accepted by the CPU, the
bytes are reset. Should the CPU not respond
immediately, the data are updated to show a
cumulative value. The mouse button is returned as
keycode dØØØ@2 Ø11Ø@2. The "d" bit defines
whether the button is pressed (1) or not (Ø).

If the mouse is plugged in, a code of 1ØØØ@2
Ø111@2 is returned. If the mouse is unplugged,
the code is ØØØØ@2 Ø111@2.

Real-Time Clock

The real-time clock (RTC) is capable of resolution
to 1/1Øth of a second and need be reset only every
16 years. An alarm can be programmed via the RTC
to generate an interrupt and/or turn the Lisa on
after a timeout of up to FFFFF@16 seconds, or
about 12 days.

The clock commands are coded as shown in Figure
2-14. The "p" bit in Figure 2-14 is used to power
the Lisa on or off under software control. A "Ø"
turns power off. The "s" bit enables and disables
Clock Set Mode.

In Clock Set Mode, only as many nibbles as are
required need be sent. Once the "s" bit is

cleared, the peripheral assumes that the data was complete. The clock and timer must be stopped while the clock is being set. The clock can be left running while setting up the timer.

Time information is entered as a series of nibbles in the form:

aaaaa y ddd hh mm ss t

The "a" nibbles are the timer delay value in seconds (0-FFFFF@16), "y" is the year (0-15), "ddd" is the day (1-366), "hh" is the hour (0-23), "mm" is the minute (00-59), "ss" is the second (0-59) and "t" is the 1/1$0$th of a second value (0-9).

All nibbles are maintained in binary coded decimal (BCD) format, except for the timer and year nibbles, which are binary. When reading the clock, the data are returned as a series of reset codes in the form:

8$0$ Ey dd dh hm ms st

Software On-Off

Software controls the on and off states in the Lisa. When the power switch on the lower-front cabinet is pressed during operation, a reset code is presented to the CPU. This allows software to finish operations in progress and store work files before turning off the Lisa. Note that pressing the on-off switch does not remove power from the Lisa; power can only be removed by unplugging the line cord.

2.5.5 Processor Board Control

The processor board has a number of control bits that are set and reset by access to a particular address in I/O space. A summary of these is shown in Figure 2-17.

Address (hexadecimal) $FC+1xx$	Function			
ØØEØØØ	Memory Diagnostic	DIAG1	Reset
ØØEØØ2	" "	"	Set
ØØEØØ4	Memory Diagnostic	DIAG2	Reset
ØØEØØ6	" "	"	Set
ØØEØØ8	Context Selection	SEG1	Reset
ØØEØØA	" "	"	Set
ØØEØØC	Context Selection	SEG2	Reset
ØØEØØE	" "	"	Set
ØØEØ1Ø	SETUP Register		Reset
ØØEØ12	" "		Set
ØØEØ14	Enable Soft Memory Error Detect		Reset
ØØEØ16	" " " " "		Set
ØØEØ18	Enable Vertical Retrace Intrpt		Reset
ØØEØ1A	" " " "		Set
ØØEØ1C	Enable Hard Memory Error Detect		Reset
ØØEØ1E	" " " " "		Set
ØØE8ØØ	Video Address Latch		
ØØFØØØ	Memory Error Address Latch		
ØØF8ØØ	Status Register		

Figure 2-17. Processor Board Control Addressing

Context selection is discussed in subsection 2.3.4.
Memory errors are discussed in section 2.7. The
status register is discussed in Section 2.8.

The video address latch is used to point to the
physical address of the 32 Kbyte video page in main
memory. The memory error address latch saves the
accessed address when a memory error occurs. This
may then be interrogated by software for statistical
analysis of memory errors.

2.6   Interrupt Handling

Upon detection of an interrupt, the CPU enters
supervisor mode automatically. It then uses a table in
memory, known as the Exception Vector Table, to point to
the location at which the routine to handle the
interrupt can be found. The priority level of the
source of the interrupt can be used as an index into the
table, or the interrupt level itself can be used
directly as the exception vector.

The fixed priority interrupts are:

Level	Type
7	Non-maskable interrupt (highest)
6	Serial I/O ports
5	Expansion slot #1
4	Expansion slot #2
3	Expansion slot #3
2	Keyboard/Mouse/Real-Time Clock/on-off switch
1	All others (lowest)

Figure 2-18 shows the Exception Vector Table assignment
for the Lisa. All addresses are logical addresses.
This means that their physical location is a function of
the MMU setup.

Exception	Vector Address (hexadecimal)
Reset: Initial SSP	000000
Reset: Initial PC	000004
Bus Error	000008
Address Error	00000C
Illegal Instruction	000010
Zero Divide	000014
CHK Instruction	000018
TRAP Instruction	00001C
Privilege Violation	000020
Trace	000024
Unimplemented Instruction 1010	000028
Unimplemented Instruction 1111	00002C
Reserved, unassigned	000030 - 00005F
Spurious Interrupt	000060
Other Internal Interrupt	000064
Keyboard Interrupt	000068
Slot 2 Autovector	00006C
Slot 1 Autovector	000070
Slot 0 Autovector	000074
RS232 Interrupt	000078
Non-Maskable Interrupt	00007C
TRAP Instruction Vectors	000080 - 0000BF
Reserved, unassigned	0000C0 - 0000FF
User Interrupt Vectors	000100 - 0003FF

Figure 2-18. Exception Vector Table

A non-maskable interrupt can come from one of four
sources:

* Power failure
* Hard memory error
* Soft memory error
* Keyboard reset.

Level-1 interrupts can be generated by one of three
sources:

* Hard disk interface, the parallel port,
* Floppy-disk controller
* Video circuit controller.

The power reset vector is not shown here because it is
located in ROM, which is not accessed except in special
I/O space during powerup processing.

2.7   Error Processing

The Lisa operates with a flexible system of handshaking
on the bus. When a device is addressed, the CPU will
wait 3Ø-3ØØ microseconds for some response from the
addressed device before timing out. Upon timeout, a bus
error is produced.

The Lisa can experience two kinds of memory errors:
hard or soft. A hard memory error is the result of a
parity error during memory access on a parity memory
board or an uncorrectable error on an Error Correction
Code (ECC) memory board.

A soft memory error is the result of detection of a
correctable error on an ECC memory board. In either
case, the appropriate status bit is set, see section
2.8, and a non-maskable interrupt is generated to the
CPU. A latch contains the address at which the error
was detected. The MMU can be used to map out bad pages
in memory, should this become necessary.

The address of the word that caused the error can be
read from the Memory Error Address Latch at ØØFØØØ@16 in
I/O space. Detection of either a hard or a soft memory
error can be disabled, as described in Figure 2-17.

Memory error address latch

```
15                      1Ø    9                                    Ø
-------------------------------------------------------------------
2Ø  19  18  17  16  15 | 14  13  12  11  1Ø  9  8  7  6 | V
```

bit Ø - Ø error on CPU access D1<-D15 contain A6-A2Ø of
              failing address

      1 - error on Video access D1Ø-D15 contain A15-A2Ø
              of failing address D1-D9 invalid

2.8   Status Register

The status register is located at ØØF8ØØ@16 in I/O space
and is a read-only 16-bit register. A bus error
exception routine can use the status register to
determine the cause of bus errors. A breakdown of the
significance of the bits in the status register is shown
in Figure 2-19.

Bit	Name	Significance
0	Soft Error	A soft memory error has occurred.
1	Hard Error	A hard memory error has occurred.
2	Vertical Retrace	The video circuit has begun a vertical retrace and an interrupt has been generated. The video circuit continues to set this bit for 90 microseconds after the start of the retrace. Enable Vertical Retrace Interrupt can be reset to inhibit this bit.
3	Bus Timeout	A timer attached to Address Strobe (AS/) waits for 30-300 micro-seconds before generating a Bus Error condition.
4	Video Bit	Available to the CPU for diagnostic purposes, this bit corresponds to the output of the video circuit.
5	Horiz. Sync	Reflects the state of the horizontal sync signal. It is available to the CPU for diagnostic purposes.
6	Video Mode	Reserved for future use.
7-15		Not used.

Figure 2-19. Status Register

CHAPTER 3. INTERNAL SPECIFICATIONS

This chapter describes specifications for the Lisa and the
manner in which it interfaces with the outside world.

3.1   Packaging

The configuration of hardware modules within the cabinet
was discussed briefly in Chapter 1. The following parts
are removeable for inspection or replacement:

   * Front panel
   * Floppy-disk drives
   * Back panel
   * Power supply
   * Motherboard
   * CPU board
   * I/O board
   * Memory boards
   * Keyboard
   * Mouse
   * Expansion boards.

Disassembly procedures for user-servicable parts are
described in the Lisa Owner's Guide. Access to other
subassemblies is described in Chapter 11.

The top front of the cabinet is taken up by the CRT and
the two floppy-disk drives. You can access these
devices by removing the front panel of the cabinet. The
drives are held in place by a finger-nut below the lower
drive, and both drives can be slid out once this is
undone. Care must be taken not to snag or overextend
the drive cables before they are disconnected from the
drives.

Removing the back panel from the cabinet gives you
access to the power supply and the motherboard
assembly. The motherboard carries all the logic boards
and conceptually consists of two parts.

The first part carries the main logic boards, including
the processor board, the I/O board, and either one or

two memory boards, parallel to the back of the cabinet.
Not all the boards are immediately visible when the back
panel is removed, because they are arranged one behind
the other.

The second part carries the boards at right angles to
the back of the cabinet, and is known as the expansion
bus section. This is where additional boards, such as
interface or controller boards, are inserted. The
entire motherboard slides out from the cabinet by gently
pulling to the rear, which disengages the two edge
connectors through which the motherboard connects into
the cabinet.

However, it is not necessary to remove the entire card
cage to remove one of the boards from the expansion
slots. These are held in place by special card-edge
connectors that allow the boards to slide out towards
the back of the cabinet.

The power supply is the rectangular enclosure occupying
the right side of the cabinet; it can be removed
separately. To do this, unfasten the finger-nut beneath
the cabinet. Then, slide the entire power supply
backwards out of the cabinet.

Electrical connections between modules and the rest of
the Lisa are made by means of tongue and socket
connectors. These connections are made automatically
when the boards are inserted and pushed home.

Only the disk drives require that their connecting cable
be carefully disconnected before the drive can be fully
removed from the cabinet. Figure 3-1 shows an exploded
view of modules inside the cabinet.

Figure 3-1. Modules in Cabinet

No module should be removed from the cabinet while the
Lisa is turned on. Interlock switches on both the front
and back panels turn the Lisa off when either panel is
removed. However, the line plug should be unplugged
before the Lisa is serviced.

The three expansion slots to the right-back of the
cabinet are designed to accept add-on logic boards.
These can be used to expand the Lisa by adding such
features as a custom interface to another computer or a
specialized controller to a peripheral that does not
readily interface with either of the ports available.
Such expansion boards must be compatible with the
specification for the expansion bus, given in section
3.4.

Expansion boards are easily removed from the Lisa with
the end-opening connectors used to house them. Turn the
lever for any slot clockwise one quarter turn, and slide
the board out of the connector.

3.2   Specifications

This section specifies environmental, electrical and
performance parameters in the Lisa. Interfaces to the
Lisa are defined in later sections of this chapter.

DUAL FLOPPY
DISK DRIVES

MEMORY
BOARDS

CPU BOARD

I/O BOARD

EXPANSION
BOARD

POWER
SUPPLY
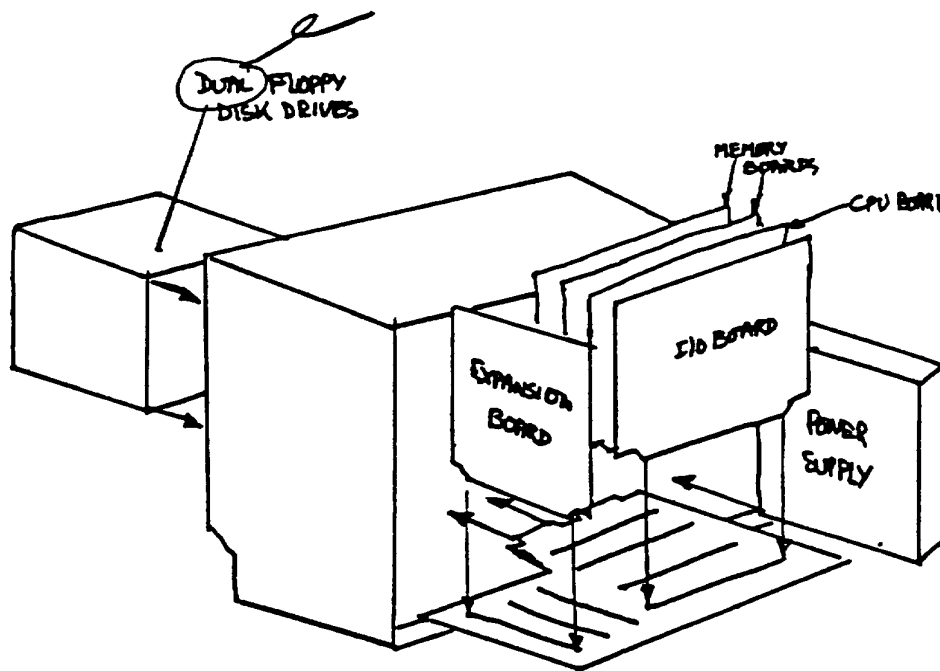
Note: All components except the disk drives
have plug-in connections.

Figure 3-1. System Component Exploded View

Modules in cabinet

3-3b

3.2.1 Environmental

The Lisa is designed to operate in an office
environment. The purpose of this section is to
define environmental limits for the Lisa which, if
exceeded, might result in a malfunction.

Note that the data apply only to the Lisa, which
includes the mouse and keyboard. Additional
equipment, such an external hard disk or printer are
specified separately in the relevant documentation.

* Operating Temperature: 0 to 35 Degrees C
* Operating Humidity: 10% to 80%
  (non-condensing)
* Storage Temperature: -20 to 70 Degrees C
* Storage Humidity: 0% to 90%
  (non-condensing).

3.2.2 Physical

Following dimensions apply to the Lisa only.

Main Assembly Dimensions:	13.9" (354 mm) High
	18.6" (474 mm) Wide
	15.6" (396 mm) Deep
Keyboard dimensions:	3.1" (79 mm) High
	18.8" (479 mm) Wide
	6.5" (166 mm) Deep
Mouse operating space:	2.1" by 6.3" (55 mm by 160 mm)
Keyboard cable extension:	4ft. (1.2 m) maximum
Main assembly weight:	44.8lbs (20.4 Kg)
Keyboard weight:	4.13lbs (1.88 Kg)
Power cord length:	7.5ft. (2.26 m)

The Lisa should be used with an acceptable operating
space around it. Under no circumstances should the
air flow through the cabinet vents, particularly
those on the bottom, be restricted.

The mouse operating space should be approximately 6
inches from either side of the keyboard. When you
move the mouse around a 6 inch area on any flat
surface, you can reach any point on the CRT with the
cursor.

3.2.3 Electrical

AC power requirements   150 VA @ 115 VAC
                                   (single phase)

                    Acceptable input voltages   90 to 130 VAC
                    Input AC frequency   60 +/- 2 Hz
                    Maximum power dissipation   150 watts @ 70 deg.F
                    Voltages available on bus   +5 V,-5 V,+12 V,-12 V,
                                                   +5 VSTBY DC

                    The currents available on these voltages (V) is a
                    function of the Lisa configuration. Refer to
                    subsection 3.3.2 for the total power capacity of the
                    power supply.

        3.3   Modules

               Each module can be easily dismounted from the cabinet
               for test or replacement. In addition, the keyboard and
               mouse detach for easy inspection or replacement. The
               Lisa consists of the following assemblies:

                   * Cabinet
                   * CRT
                   * Power supply
                   * Motherboard
                   * Two floppy-disk drives
                   * Video board
                   * Processor board
                   * I/O board
                   * 2 memory boards (maximum)
                   * Keyboard
                   * Mouse
                   * Switch/Disk cable
                   * Power supply harness.

               Refer to Chapter 11 for details on the assemblies.

               3.3.1 Cabinet

                    The cabinet consists of the sheet-metal frame and
                    the plastic cladding parts. In addition, the
                    following modules are not easily accessed and can be
                    considered as a part of this assembly.

                        * CRT assembly
                        * On-off switch board
                        * Disk-cable harness
                        * Power-supply harness.

                    The general view of the cabinet assembly is shown in
                    Figure 3-2.

Figure 3-2. Cabinet Assembly

3.3.2 Power Supply

The power supply is a self-contained unit, located
in the right back of the cabinet. The supply weighs
approximately 3.5 pounds and provides the following
voltages:

```
        +5 V    @    8.0 Amps (A)
        -5 V    @    0.2 A
       +12 V    @    2.0 A
       -12 V    @    0.2 A
       +33 V    @    0.6 A
      +5 STBY   @    0.1 A
```

3.3.3   Floppy-Disk Drives

The floppy-disk subassembly consists of two
floppy-disk drives in a sheet-metal carrier. The
carrier is installed by sliding it into the
upper-right front of the cabinet. Before the drives
are inserted, the disk cable must be connected to
the back of both disk drives in the assembly. The
longer cable goes to the upper drive.

The assembly is held in place by a finger screw. It
can be accessed by removing the front panel of the
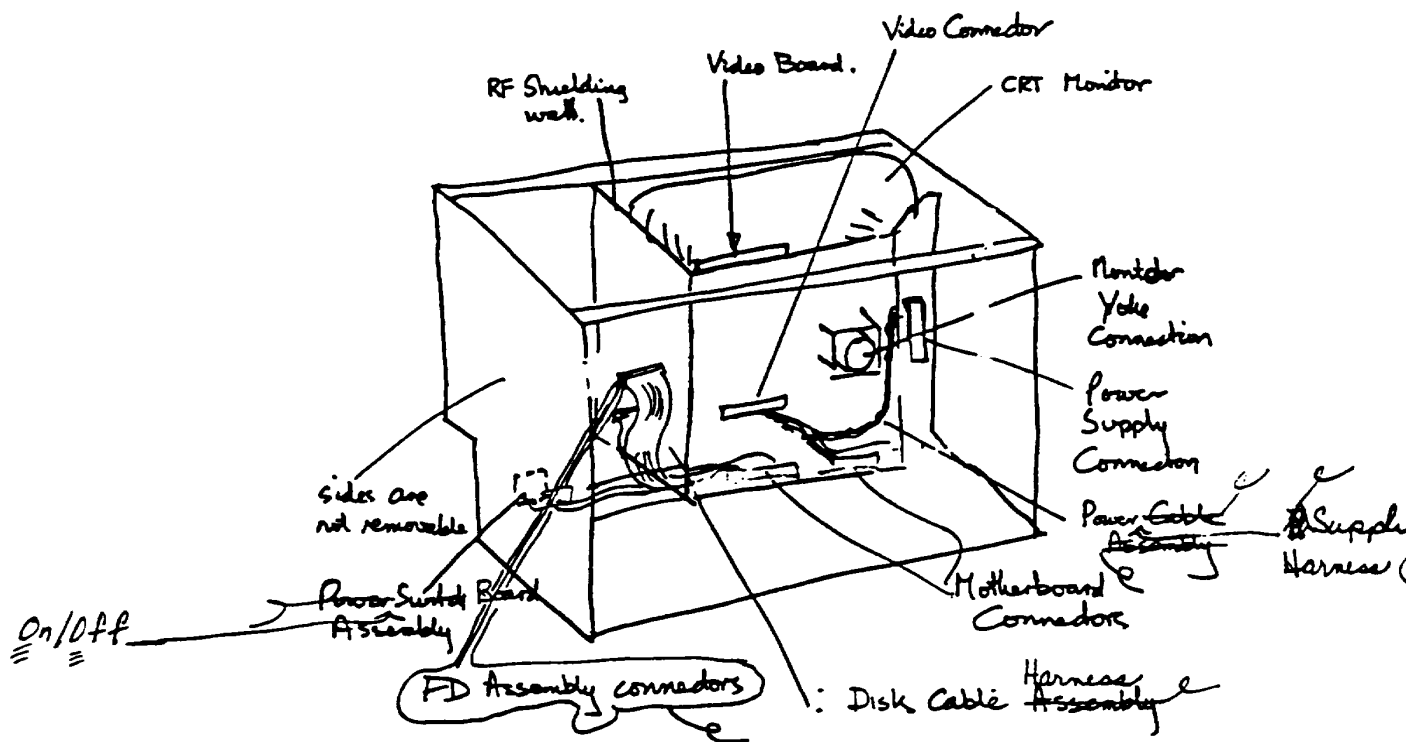
Figure 3-2. Main Chassis Assembly

3-6b

cabinet.

3.3.4 Printed Circuit Boards

The circuit boards are keyed such that it is not
possible to insert a board into the wrong slot. For
this reason, care should be taken not to force a
board into a slot. The extraction handles of all
logic boards in the Lisa are color-coded to
illustrate the correct slot and orientation.

3.3.5 Keyboard and Mouse Assemblies

The keyboard stands alone and connects to the switch
assembly in the lower-right corner of the cabinet.
It receives its power input from, and transmits key
data over, this cable. The keyboard assembly
consists of a single printed circuit board (PCB)
that carries all keys and logic components
sandwiched between the two halves of the plastic
housing.

The mouse stands alone and connects to the special
9-pin DB connector at the center-back of the
motherboard.

3.4   The Expansion Bus

A subset of the internal system bus is made available on
three slots in the motherboard. These are accessible
from when the back panel is removed from the cabinet.
They are equipped with end-opening connectors, which
allow expansion PCBs to be inserted or removed without
removing the motherboard from the cabinet. However, the
AC line cable should be disconnected whenever an
expansion board is being removed or inserted.

The purpose of this section is to provide a
specification of the expansion bus and its physical
configuration to permit an interface to be designed that
will plug into the expansion bus.

Software to handle such a component must also be
generated. The generation of such software lies beyond
the scope of this manual. Refer to Chapter 2 and to the
documents listed in the Preface for assistance.

3.4.1 Bus Signal List

The expansion bus is an extension of the system
bus. It provides sufficient data, address and
control lines to enable peripherals, in addition to
those implemented on the processor and I/O boards,
to operate within the Lisa environment.

Many signal names are recognized as corresponding to
those available on the 68000 processor chip. In all
such cases, these are simply buffered versions of
the 68000 signal, with the function being identical
to the original. Refer to the 68000 User's Manual
for details of individual signals.

Other signals, such as the slot high and low decode
signals, are generated or received by the processor
board logic. A diagram of the signal layout on the
connector is shown in Figure 3-3.

```
                           Front of the Lisa
                         -------------------
            +5 V    |  56  |  55  |  +5 V
   Digital Ground   |  54  |  53  |  Digital Ground
       +5 Stdby     |  52  |  51  |  SPKRIN
            UDS/    |  5Ø  |  49  |  LDS/
            READ    |  48  |  47  |  AS/
           DTACK/   |  46  |  45  |  +12 V
            VPA/    |  44  |  43  |  VMA/
            BA12    |  42  |  41  |  BA11
            BA1Ø    |  4Ø  |  39  |  BA9
            BA8     |  38  |  37  |  BA7
            BA6     |  36  |  35  |  BA5
            BA4     |  34  |  33  |  BA3
            BA2     |  32  |  31  |  BA1
            BDØ     |  3Ø  |  29  |  BD1
            BD2     |  28  |  27  |  BD3
            BD4     |  26  |  25  |  BD5
            BD6     |  24  |  23  |  BD7
            BD8     |  22  |  21  |  BD9
            BD1Ø    |  2Ø  |  19  |  BD11
            BD12    |  18  |  17  |  BD13
            BD14    |  16  |  15  |  BD15
          BGOn-1/   |  14  |  13  |  BGOn/ (n=slot #)
            BR      |  12  |  11  |  E
           BGACK/   |  1Ø  |  Ø9  |  LDMA/
           CPUCK    |  Ø8  |  Ø7  |  RESET
           IAKn/    |  Ø6  |  Ø5  |  INTn/
            SHn/    |  Ø4  |  Ø3  |  SLn/
           -12 V    |  Ø2  |  Ø1  |  -5 V
                         -------------------
                           Back of the Lisa
```

Figure 3-3. Signal Pin Layout

3.4.2   Bus Signal Descriptions

BDØ-BD15   16 buffered data lines that comprise the
           data bus.

BA1-BA12   12 buffered address lines that select one
           of 4Ø96 words. Since the lines are
           derived from the low-order 12 lines from
           the MMU, a process which is assigned a
           segment enclosing the 16384 bytes on an
           expansion card can address the I/O card
           from Ø-3FFF@16.

AS/   A signal that is the address strobe, which
           indicates that the CPU has initiated a
           memory cycle. Due to the MMU delay on the
           processor board, only bits BA1 to BA8 are
           definitely stable at this time; the
           high-order 4 bits may still be changing.

UDS/   Upper Data Strobe indicates that, during a
           write operation, the upper byte on the bus
           (BD8-BD15) is valid in the current bus
           cycle.

LDS/   Lower Data Strobe indicates that, during a
           write operation, the lower byte on the bus
           (BD0-BD7) is valid in the current bus
           cycle.

DTACK/   Data Transfer Acknowledge indicates to the
           CPU that the expansion device has
           performed whatever data transfer had been
           requested by the CPU and that the current
           cycle can be completed.

READ   This signal indicates the direction of
           data transfer to be performed on the
           buffered data lines. The signal being
           asserted indicates that the CPU expects
           the I/O device to present data on the
           bus.

VPA/   Valid Peripheral Address indicates to the
           CPU that the device currently being
           addressed operates with a 6800-compatible
           bus cycle. VPA/ must never be asserted
           concurrent with DTACK/.

VMA/   Valid Memory Address signals the
           peripheral that the CPU has recognized the
           VPA signal and is now executing a 6800
           cycle.

E   Equivalent of the 6800 phi2 clock. It is
           high for 4 clock cycles and low for 6,
           giving E a frequency of 500 kilohertz
           (KHz) in the Lisa.

BR/   Bus Request tells the processor that a
           peripheral device is requesting control of
           the bus.

BGOn/   A Bus Grant-input is issued by the CPU
           once a direct memory access (DMA) device
           has been given control of the bus. If the

                                expansion card had requested the bus, this signal allows the card to assume control of the bus. Otherwise, the BGOn-1 pin is used to daisy chain grants to the near slot. Note that the 68000 bus master protocol is used.

BGOn-1/	A Bus Grant-output that reflects the condition of BGOn if the peripheral does not wish to use the bus. The connections from BGOn to BGOn-1 must not be altered during a DMA cycle.
BGACK/	Bus Grant Acknowledge; driven by the expansion card when it assumes control of the bus and is deasserted only when it wishes to relinquish control.
LDMA/	Load DMA; used to load the high address of the DMA latch. Due to the number of bus lines available, the high 8 address bits are latched on the CPU board from the contents of the 8 data bits BD5-BD12. The expansion device must control both the signal and the contents of the latch, which must be loaded at the beginning of any DMA transfer.
CPUCK	A buffered 5 MHz CPU clock, which is available for general timing use.
RESET/	Signal asserted by the CPU board, which makes all peripheral devices return to their power-on state. If the Lisa is off and RESET is pulled to +5Stdby with a 100 ohm resistor, the Lisa turns on.
+5Stdby	A +5.7 V source that is available whenever the Lisa is attached to an AC supply. Note that while this suppply is available when the Lisa is off, it is not battery backed-up and therefore is not present when the Lisa is unplugged. No more than 40 milliamps (mA) should be drawn from this supply.
INTn/	Signal used by the expansion device to interrupt the CPU. It should be held asserted until the interrupt is acknowledged from the CPU.
IAKn/	Signal used to acknowledge an interrupt made by a peripheral device.

> SLn/   Signal used by the CPU to select the
>   low-order contiguous 4096 words on the
>   expansion device that are addressed by
>   BA1-BA12.
>
> SHn/   Signal used by the CPU to select the
>   high-order contiguous 4096 words on the
>   expansion device that are addressed by
>   BA1-BA12.

3.4.3 Bus Parameters

The expansion bus provides five DC voltages to
devices that may be connected there. The total
current that can be drawn on them for all devices
connected to the bus is as follows:

+5 VDC	2.0 A
-5 VDC	0.075 A
+12 VDC	0.83 A
-12 VDC	0.1 A
+5 VSTBY	0.040 A (always available)

The +5 VSTBY voltage is at a level of 5.7 V whenever
AC power is applied to the Lisa. The mechanical
layout of an expansion board must conform to Apple
Specification #062-0143.

All signals on the expansion bus are
Transistor-Transistor Logic (TTL). Drivers to the
bus are of the following types:

BA1-BA8	LS244
BA9-BA12	LS374/LS373
BD0-BD15	LS245
SHn,SLn	LS138
BGOn, ...	Depends on next board
UDS,LDS,AS,READ,VMA,E	LS244
BGACK	F02
RESET	7417 (wired OR)
IAKn	LS156

All signals with an "n" are unique to the slot being
used and need not be buffered. All other signals
should be buffered on the expansion board to
minimize loading on the bus itself.

Signals not mentioned above are input to the bus
from the expansion board. A bus driver device
should drive these.

3.4.4 Bus Timing

Timing on the expansion bus closely follows that of
the 68ØØØ CPU device. Refer to the 68ØØØ User's
Manual for details.

Expansion bus timing is controlled by the slot
decode signals from the processor board and by the
acknowledge signal from the controller on the
expansion bus. Since the expansion bus is merely an
extension of the system bus, signal timing is
identical on both.

Normal data transfer on the bus begins with the
address strobe signal being asserted. At this time,
the bus address lines are not valid because of time
delays in the MMU. The slot decode signal to
asserted during the S5 state of the processor cycle
after the address and data strobe lines are stable.

The signal sequence for a read operation from the
expansion bus by the CPU is shown in Figure 3-4.
The CPU waits for the DTACK/ signal from the
addressed expansion peripheral before completing the
cycling by reading the data from the data bus.
Should the peripheral not respond, the CPU times out
after approximately 3Ø milliseconds with a bus error
condition. This is shown in the first cycle of
Figure 3-4.

```
                          Min  !    Max
                               !
                     ──────────!──────────
                               !
        Cycle time   8ØØns  !  3ØØus
        TAsetup      1ØØns  !   ──
        TDsetup      1ØØns  !   ──
        Tfinish      1ØØns  !  26Øns
```

Figure 3-4. Expansion Bus Read-Timing Diagram

Data transfer from a 68ØØ-type peripheral is
performed with the assistance of the VMA and VPA
handshake signals, plus the E clock signal. These
signals are described in the signal list above and
in the 68ØØØ User's Manual. The transfer cycle is
similar to a normal data transfer with the VPA and
VMA signals operating as handshake signals instead
of SLn and DTACK.

Data are written to a peripheral in a similar
manner. The slot decode being asserted indicates
that valid data are being presented to the bus by
the CPU. The DTACK signal acknowledges receipt of
the data. This is shown in Figure 3-5, along with a
68ØØ-type write cycle.

Expansion peripherals normally use the slot decode
to drive the acknowledge signal. Any peripheral
using DMA must follow the timing described in the
68ØØØ User's Manual.
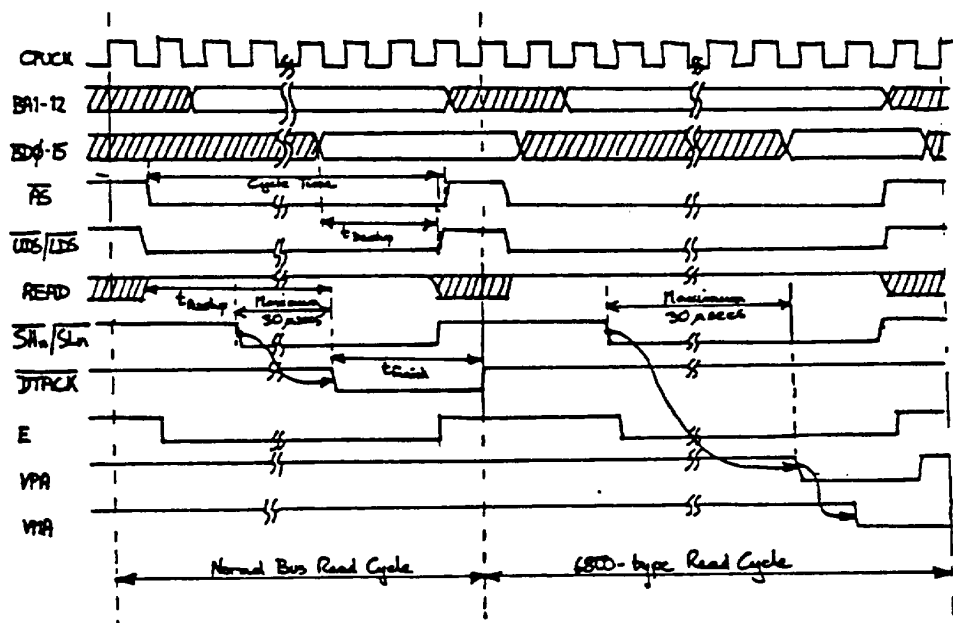
	Min !	Max
Cycle time	800ns !	300us
TAsetup	100ns !	--
TDsetup	100ns !	--
Tfinish	100ns !	260ns

Figure 3-4. Expansion Bus Read Timing Diagram

3-14b

Figure 3-5. Expansion Bus Write Timing Diagram

3.4.5 DMA Scheme

The DMA scheme used in the Lisa corresponds closely
with that used in the 68000 CPU. The BG lines are
daisy chained on the motherboard. The priority
assigned to an expansion device is therefore a
function of the interface design and the choice of
physical location of the card in the expansion
slots.

The hardware priority for DMA devices is:

         Highest   I/O Board
                        Slot 3
                        Slot 2
         Lowest   Slot 1

In order that the priority chain is not interrupted,
any card that does not use DMA must hard wire its
BGOn signal to BGOn-1 signal.

Since this propagation will not occur if no card is
present, it is essential that the slots using DMA
are filled beginning with slot 3.
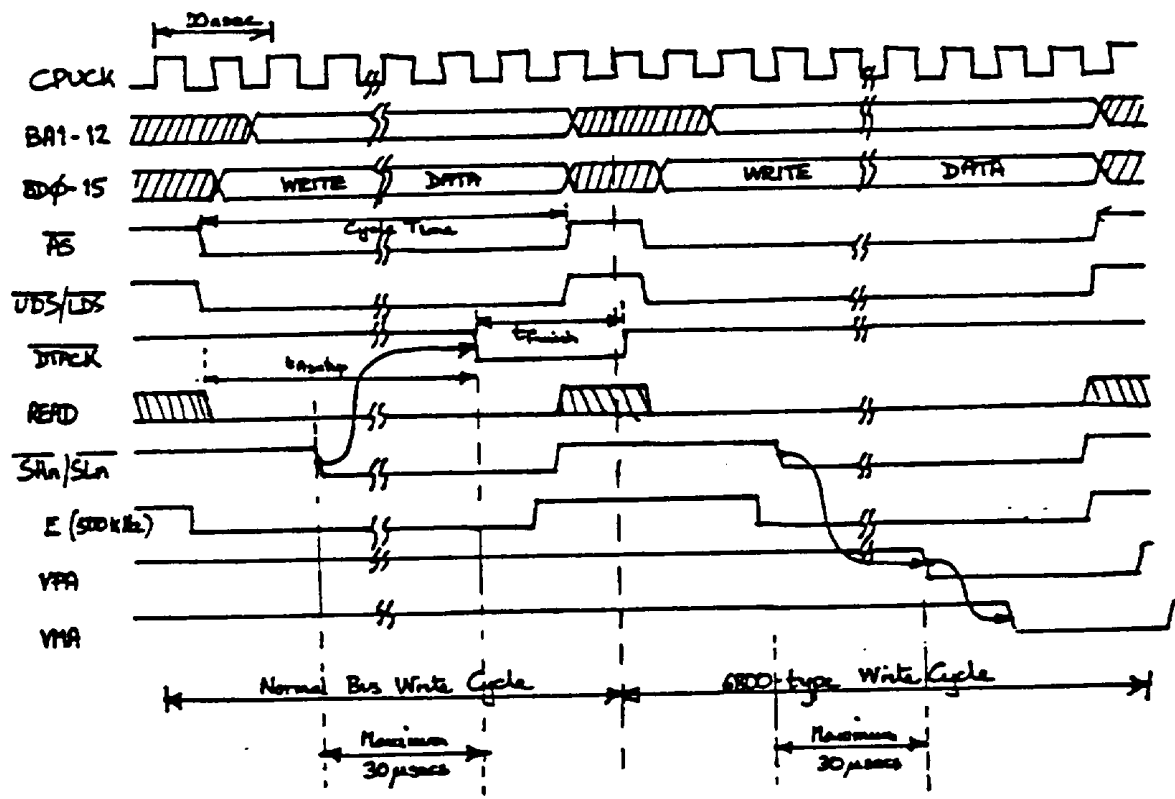
Figure 3-5.   Expansion Bus Write Timing Diagram

3-15b

DMA transfers should be limited to 1 millisecond in
order not to interfere with the processor's ability
to proceed with normal program execution.

In addition to those lines mentioned in subsection
3.4.2, an expansion device that uses DMA must also
be capable of driving the following signals:

  * All 16 data lines
  * All 12 address lines
  * AS/ , UDS/ , LDS/ , and READ.

Timing of these signals should follow those
generated by the 68000 as given in the 68000 User's
Manual and in Figures 3-4 and 3-5. Note that DMA
accesses use physical address.

The high-order 8 bits of the DMA address are held in
a latch located on the processor board. This latch
must be loaded by asserting the desired byte on
BD5-BD12 and asserting LDMA/ before any transfer is
attempted.

3.4.6 Bootstrap Protocol

If an expansion device is to be used to boot the
operating system at power-on time, it must be
self-identifying and an identification protocol must
be followed.

Each device must contain ROM storage, the contents
of which must be programmed to include the
information shown in Figure 3-6. The byte-wide ROM
contains word data stored with the low byte
following the high byte.

*Note: Expansion Card ROM is on
the lower half of data bus.

Therefore, ignore MSB of
each read 16-bit word.*

MSB   LSB

X   used

```
         Address           Contents

                     +----------------------+
            1        !     Type Code       !
                     +----------------------+
            5        !     Word Count       !
                     +----------------------+
            9        !Status routine entry !
                     +----------------------+
            13       ! Boot routine entry  !
                     +----------------------+
            17       !     Icon Pointer    !
                     +----------------------+
            21       !                      !
                     !     Program data     !
                     !          and         !
                     .     icon bitmaps     .
                     .                      .
                     .                      .
                     !                      !
                     +----------------------+
            nn       !      Checksum        !
                     +----------------------+
```

Note: Addresses as accessed by the Lisa.

Figure 3-6. Bootstrap ROM Format

The first word of the ROM defines a type code. This
code is a 16-bit number with the most significant
byte in location 1 and the least significant byte in
location 3. It has the following form:

          bsit@2 nnnn@2 nnnn@2 nnnn@2

where b = 1 if device is bootable
      s = 1 if device has status program
      i = 1 if device has an icon(s) to be displayed
      t = 1 if device is a test card
      n = device (or board) identification number

If the expansion device is selected for booting, the
boot ROM first checks that the card is bootable by
checking the "b" bit. If this bit is not set to a
1, the boot is aborted and the boot ROM displays an
error to the user.

If the status bit is on, the boot ROM first executes
the status program by using the status routine entry

pointer. In addition, when the expansion device is
selected, the status routine is executed again. The
boot ROM preloads Register A1 with the address of
the expansion slot's low select (SLn) to enable the
status and boot programs to access the device by
addressing relative to A1. The status program must
always return to the boot ROM with the result in
register D$\emptyset$ via a return to subroutine (RTS)
instruction. A status of $\emptyset$ indicates that all is
well, while a nonzero status aborts the boot and the
boot ROM displays an error to the user.

The icon pointer provides a method for expansion
devices to display to the user a boot option in a
pictorial manner. If the icon bit is set to a 1,
the boot ROM scans the expansion device ROM using
the icon pointer and expects the following format:

        Icon Pointer (one word) - points to:

        Icon count (one byte up to two icons)
        Pointer to first icon (word)
        Pointer to second icon (word)
        First icon (bitmap)
        Second icon (bitmap)

The icon pointer must be a one-word value containing
the byte offset from the base ROM address to the
byte containing the icon count. The pointers to the
actual icon(s) must also be in this format. The
icons themselves can be stored in a compressed
manner, and, if so, the icon count byte must have
its most significant bit (MSB) = 1 with the
remainder of the byte being the actual count. The
compressed format must be the same as that used by
the boot ROM; a special program is currently
available to do the compression. If not compressed,
the icon(s) must be standard 48 by 32-bit Lisa
icons, and should be stored as 32 horizontal rows of
6 bytes each, 192 bytes total.

If the user requests the boot icon menu at power-up
time, the boot ROM will display the standard boot
icon options along with the expansion-device icons,
if present. Up to two icons can be displayed per
expansion device, and the boot ROM will assign them
unique boot id's as follows:

```
        I/O Slot        Boot id's

           1            3,4
           2            6,7
           3            9,A
```

If an expansion-device icon is selected for booting,
the boot id will be relayed to the loaded boot
program in register D∅.

The test card bit is primarily intended for internal
use by Apple manufacturing. The Lisa boot ROM makes
two special checks if an I/O slot card is installed
with the test card bit set:

1. If no other cards are installed, the test
    card id is in the range 0@16 to 77F@16,
    and the boot bit is set, the Lisa
    defaults to booting from the test card.

2. If the test card id is in the range 0@16
    to 7F@16 and an Applenet card is also
    installed, the Lisa defaults to booting
    from the Applenet card.

The final two parameters in the expansion device ROM
are the word count and checksum. The word count
should be a 16-bit number indicating the length in
words of the ROM data starting from the status
routine entry point up to, but not including, the
checksum word. The boot program will be read into
memory starting at address ∅2∅∅∅∅2 as 16-bit words.
As the words are loaded they will be added to a
cumulative 16-bit sum, which is rotated to the left
one bit position after each add. The 2-byte
checksum should produce a ∅ result when added to
this calculated sum and all the rest of the data in
the ROM, including the type code, routine entry
points, icon pointer, word count and icon bitmaps.

3.5   The External Ports

The Lisa is equipped with several standard interfaces
for additional devices, such as printers and hard disks,
that can be attached. This section provides a
convenient specification for these interfaces.

The external plugs and sockets available are:

   * 2 serial RS232-C ports
   * 1 25-pin DB parallel port

* 1 9-pin DB mouse connector
* 1 3-pin keyboard connector
* 1 co-axial composite video jack.

3.5.1 Serial Port Interface

The two built-in RS232-C serial communication ports
can support local asynchronous communication at
rates up to 19.2 kilobaud (Kbaud). In addition,
port number 1 conforms to RS232-C type-D
specifications, which enables full modem control
with either synchronous or asynchronous protocols.

The pin assignments and their use on both ports are
shown in Figure 3-7. Both channels are set up to be
the data terminal equipment (DTE) end of the
communications system.

In order to connect other DTE equipment, a modem
eliminator or "null modem" is required. An Apple
null modem (59Ø-ØØ29-ØØ) with a communication card
cable can be used to connect a serial printer to the
Lisa via a serial port. Both ports are standard
25-pin D-type female connectors.

Signal Name	Description	Channel A	Channel B
TxD	Transmit Data	2	2
RxD	Receive Data	3	3
RTS	Request to Send	4	4
CTS	Clear to Send	5	n/a
DTR	Data Terminal Ready	2Ø	2Ø
DCD	Data Carrier Detect	8	n/a
TxC	Transmit Clock Input	15	n/a
RxC	Receive Clock Input	17	n/a
TEXT	Transmit Clock Output	24	n/a
DSR	Data Set Ready	n/a	6
RxD	Applebus Receive Data	n/a	19

Note: n/c = not connected.

Figure 3-7. Serial Port Pin Assignments

3.5.2 Parallel Interface Port

This interface is normally used to connect a hard
disk, such as the Apple Profile to the Lisa. It may

alternatively be used to connect a device that has a
high data transfer rate and for which the serial
ports are not appropriate.

The port is a general-purpose 8-bit interface that
is presented on a 25-pin D-type connector. Pin 7 is
blocked to prevent connection of an RS232-type
cable. The pin assignments are shown in Figure
3-8.

```
                        __
                       |   \
                       |    \
         Ground   |  1   \
                       |   14  |   Ground
         Ground   |  2      |
                       |   15  |   PSTRB/
          DR/W/   |  3      |
                       |   16  |   BSY
         Ground   |  4      |
                       |   17  |   CMD/
           DD0    |  5      |
                       |   18  |   PARITY/
           DD1    |  6      |
                       |   19  |   OCD
       (blocked)  |  7      |
                       |   20  |   Ground
           DD2    |  8      |
                       |   21  |   CRES/
         Ground   |  9      |
                       |   22  |   DD3
         Ground   | 10      |
                       |   23  |   DD4
           DD5    | 11      |
                       |   24  |   Ground
           DD6    | 12      |
                       |   25  |   CHK
           DD7    | 13    /
                       |     /
                       |__  /
```

Figure 3-8.   Parallel Port Pin Assignments

The meaning of the individual signals on the
interface is as follows:

DD0-DD7   Eight bidirectional data lines. Bit DD7
           is the MSB.

DR/W/   A line driven high by the Lisa to indicate
          that data are expected to be input on the
          data lines. It is driven low to indicate
          that data are being output.

PARITY   Bidirectional line that must be configured
          on the basis of the data currently on the
          data lines to give odd parity.

PSTRB/   Processor strobe line used as a signal by
          the Lisa to indicate valid data being
          output.

CMD/   A line asserted by the Lisa to indicate
          that a command has been placed on the data
          lines.

BSY/   A line asserted by the peripheral to
          indicate to the Lisa that it is busy and
          unable to process commands on the
          interface.

OCD   A line monitored by the Lisa. If it is
          high, it is assumed that no device is
          connected to the interface.

CRES/   A line asserted by the Lisa when the
          peripheral is to be reset to its power-on
          state.

CHK   Signal that may be used to interrupt the
          CPU in the event that a fault condition
          has occurred in the device connected to
          the interface.

3.5.3 The Mouse Interface

The mouse is connected to the Lisa by means of a
9-pin DB connector, located in the middle of the
connector panel at the back. The connector pin
assignment is shown in Figure 3-9.

```
                              _
                             |  \
                             |   \
               Switch 1  | 1      \
                             |   6  |  Switch 2
                  +5 V  | 2       |
                             |   7  |  Button
               Ground  | 3       |
                             |   8  |  Down
                 Left  | 4       |
                             |   9  |  Up
                Right  | 5      /
                             |      /
                             !_  /
```
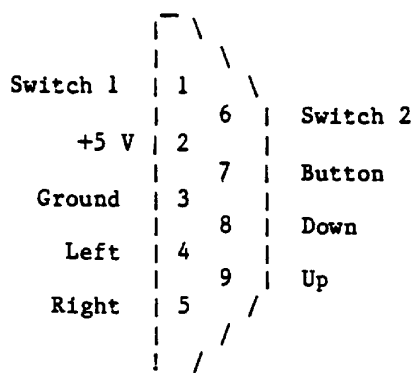
Note: Switch 2 is connected to CHK on the parallel port.

Figure 3-9. Mouse Interface Pin Assignment

3.5.4 The Keyboard Interface

The keyboard interface consists of a 1/4 inch stereo
phone jack connector. It is defined as follows:

```
          Ring      Data
          Shield    Ground
          Tip       +5 V
```


3.5.5 Composite Video Interface

This interface consists of a phone jack at the back
of the cabinet. It is available to drive an
external CRT monitor.

The signal levels conform to RS170. The horizontal
sweep rate is 22,400 Hz and the vertical refresh
rate is 60 Hz.

CHAPTER 4. THE PROCESSOR BOARD

_____

The heart of the Lisa is the processor board. It contains the
following major logic components:

* Central processing unit (CPU)
* Memory management unit (MMU)
* Timing generation
* Memory timing
* Video generation
* Interrupt control
* I/O decode
* Direct memory access (DMA), error address, and flag
  latches.

The processor board is so called because it contains the logic
associated with the 68000 CPU. It also contains the main
memory management and bus control functions for the Lisa.
Some additional circuitry, such as error latches and video
control, are also located on this board for convenience.

The function of the processor board is to execute the Lisa
software, provide main timing for communication within the
Lisa, and to provide additional control functions for the
video logic.

4.1   Processor Board Block Diagram

An overview of how the components on the processor board
logically interact is shown in Figure 4-1. Refer also
to Figure 1-2 in Chapter 1, which gives an overview of
the Lisa in block diagram form.

Figure 4-1. Processor Board Block Diagram

The processor board is capable of performing a number of
operations that involve data flow within the board.
Since both processor and video memory cycles are
interleaved within one machine cycle, this leads to two
major data paths during operation. Additionally, data
transfer to and from peripheral devices during normal or
DMA cycles gives rise to two other cycles, plus the path
that loads the DMA address latch.

Addresses generated by the CPU are translated from
logical to physical addresses by means of the MMU. A
discussion of MMU programming can be found in section
2.3. Addresses generated by the video or the DMA logic
are not subject to translation, i.e., they are physical
addresses.

ROM provides non-volatile storage that is used during
power-up initialization for bootstrap of the operating
system. It can be addressed either with or without use
of the MMU.

Internal timing on the board and on the bus conforms to
the timing requirements of the 68000, as described in
the 68000 User's Manual. Operation of RAM memory is
controlled by additional timing logic on the processor
board.

The data-flow paths within the processor board are
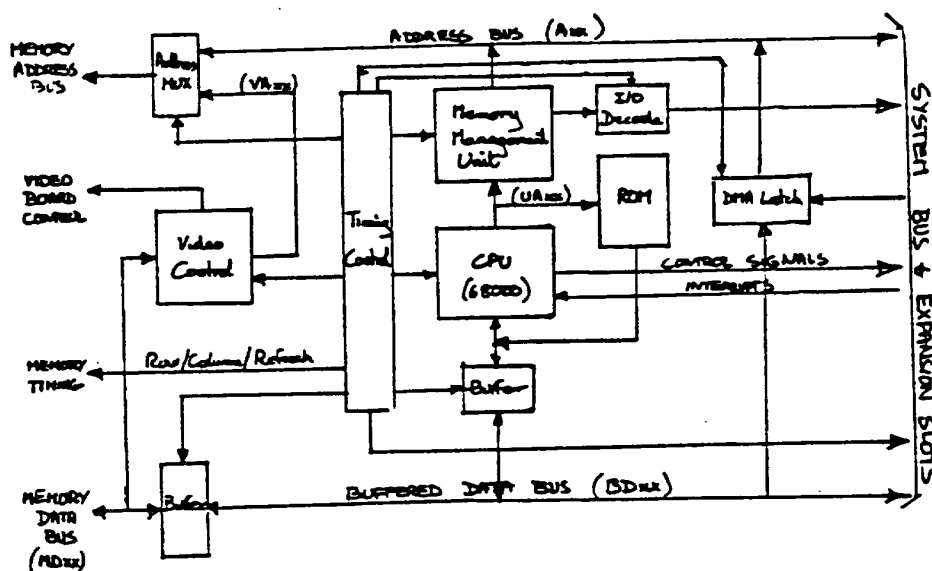
LISA Hardware Manual

Figure 4-1. Processor Board Block Diagram

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4-2b

classified as follows:

* CPU memory access
* Video memory access
* CPU access to I/O
* I/O access to the DMA address latch
* I/O access to memory.

Video memory access and I/O memory access can occur
simultaneously because of the separation of the control
lines and data paths involved. These classes are
discussed in the following subsections.

4.1.1 CPU Access to Memory

CPU and video memory cycles are interleaved on the
memory bus. Every memory cycle takes 400 ns. A
video cycle occurs every 800 ns; a CPU cycle can
occur between any two view cycles. The paths used
in memory access are shown in Figure 4-2.

The CPU generates the 24-bit logical memory address
during the previous video cycle. This address is
presented to the MMU, which performs access checks
and address translation in time to present a
physical address to the memory board at the
beginning of the CPU memory cycle.

The buffered data bus is used to transfer data
between memory and the CPU under control of bus
signals manipulated by the CPU.

Figure 4-2. CPU Access to Memory

4.1.2 Video Access to Memory

The video cycle is used to access the bit-mapped
display data located in main memory. The paths used
by the video control to access memory data are shown
in Figure 4-3.

The video control generates physical addresses that
are presented to the memory addressing multiplexer
on the processor board for direct access to the
memory location. Data that is read out of memory in
this way is presented to the video control via the
memory data bus.

Figure 4-2. CPU Access to Memory

4-4b
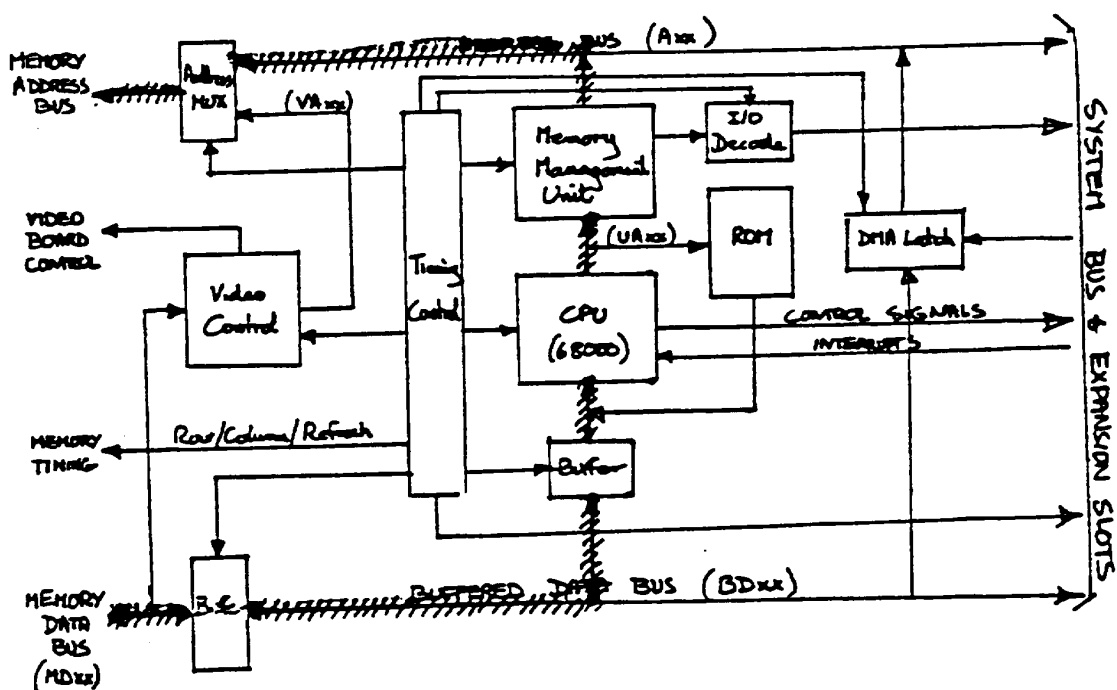
Figure 4-3. Video Access of Memory

4.1.3 CPU Access to I/O

The CPU communicates with I/O over the system bus.
I/O can be a device either located on the I/O board,
which is always resident, or can be located on an
expansion board in one of the expansion slots.

The CPU generates the logical address of the I/O
device with which it wishes to communicate and
presents it to the MMU in a manner similar to a
normal memory access.

Within the MMU, the SLR contains information that
defines the segment being accessed as valid I/O
space. This condition inhibits any memory access
and instead presents the address generated by the
MMU to the I/O decode logic.

The I/O decode logic generates an enabling signal to
the board on which the device is resident, and the
data transfer takes place via the system bus. Refer
to Figure 4-4 for an overview of the paths taken.

Note that this cycle can be simultaneous with an
access to memory by the video control, since no
logic or data path is common to both.

Figure 4-3. Video Access of Memory

Lisa Hardware Manual

Figure 4-4. CPU Access to I/O

4.1.4 I/O Access to DMA Address Latch

Transfer of data between main memory and I/O devices
in the Lisa can take place under DMA control. This
relieves the CPU from involvement in the transfer of
every byte to and from the peripheral.

In order to generate the required physical addresses
and to present them to memory, the processor board
is equipped with a latch to hold the high-order byte
of the memory address. When the high-order byte is
to be changed to allow access to another block, the
DMA controller can load the latch as shown in Figure
4-5.

Note that this operation does not require use of the
memory bus and can therefore proceed in parallel
with a video access to memory.

LISA Hardware Manual

Figure 4-4. CPU Access to I/O

|
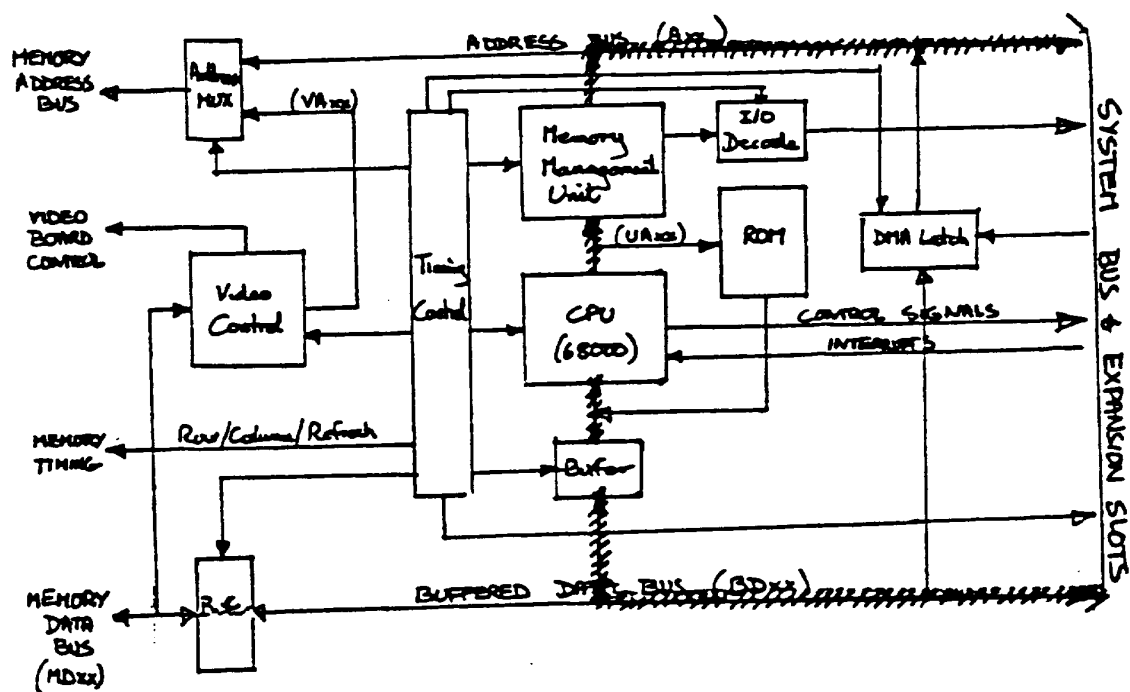
April 1983   Lisa Hardware Manual

Figure 4-5. I/O Access to DMA Address Latch

4.1.5 I/O Access to Memory (DMA)

As discussed in the previous subsection, the Lisa
can use DMA to transfer data between memory and
peripherals in a manner transparent to the CPU. The
paths used to perform this are shown in Figure 4-6.
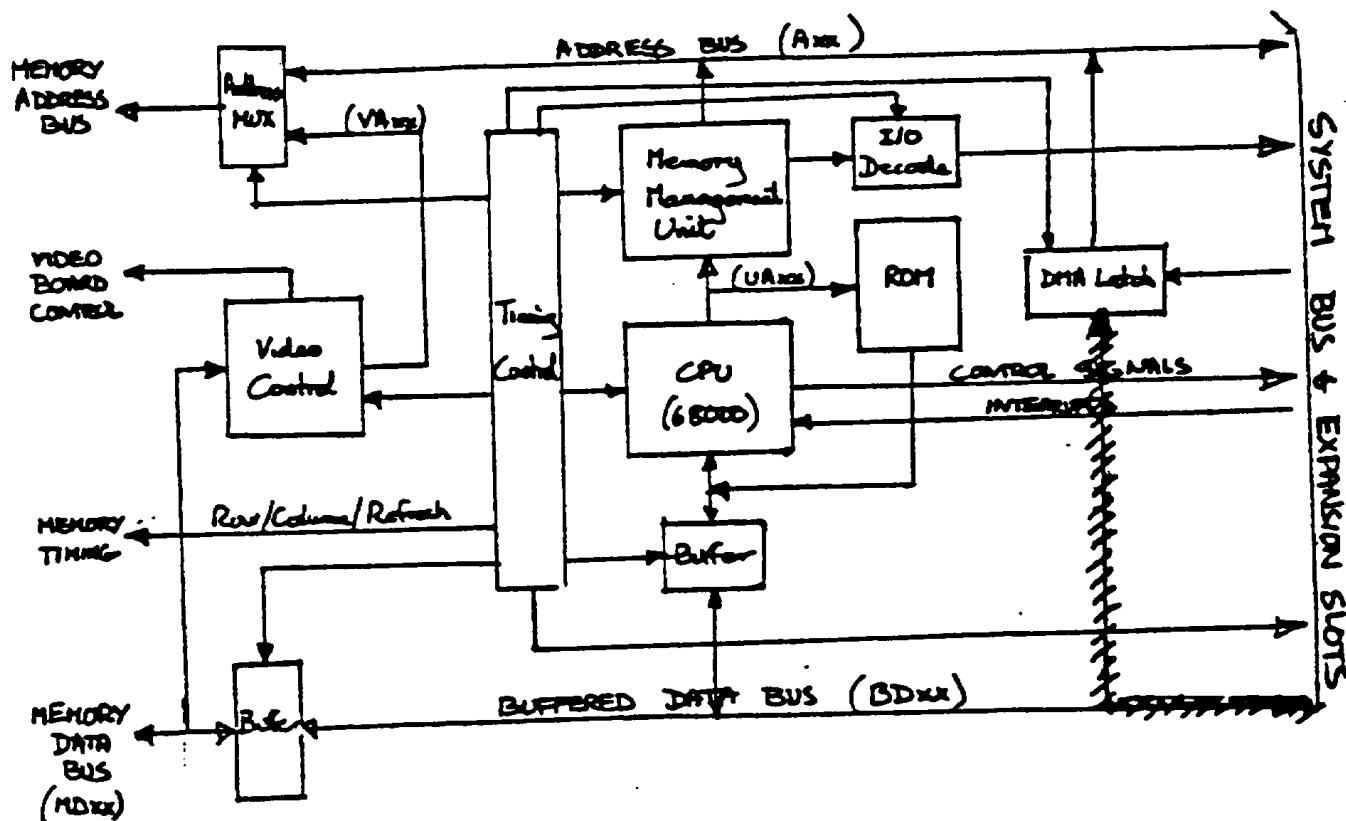
Figure 4-5. I/O Access to DMA Address Latch

Figure 4-6. I/O Access to Memory (DMA)

A physical memory address is generated by the DMA
controller from the DMA address latch contents for
the high-order byte and address lines A1-A12 to give
the full address.

This address is presented to the memory in a manner
identical to a normal CPU access, and the data are
transferred via the buffered data bus.

No other data transfer can take place during this
portion of a DMA cycle. Each series of DMA cycles
begins with a procedure in which the CPU
relinquishes control of the bus. From this time,
all signals on the bus that are required for data
transfer are generated by the DMA controller.

It is important that the design of I/O cards that
use DMA takes into consideration the overall timing
and software constraints as described in section
4.2. Since the CPU is not processing instructions
at this time, the I/O card "replaces" the CPU and
must generate signal patterns that are
indistinguishable from those of the CPU.

Figure 4-6.   I/O Access to Memory (DMA)

4-11 8b

4.2   Instruction Cycle and Timing

Apart from internal signals used on the board itself,
the main signals generated by the processor board are
used to control timing to the memory array, data refresh
on the CRT screen via the video control, and data
transfer on the system bus.

4.2.1   Internal Timing

The timing internal to the processor board is based
on the timing of the 68000. The basic 800 ns 68000
bus cycle is divided into two equal halves. A 400
ns video cycle is followed by a 400 ns processor
cycle.

A timing diagram of the principal signals internal
to the processor board is shown in Figure 4-7.

Figure 4-7. Processor Board Internal Timing

Each half of the instruction cycle is in turn
divided into eight timing periods t0 through t7,
each of 50 ns. These periods are generated by a
20.375 MHz signal called DOTCK. DOTCK is divided by
four to provide the 5 MHz CPUCK signal used to
clock the 68000. The processor board synchronizes
to the 68000 so that the S- states of the 68000

September 7th 1982
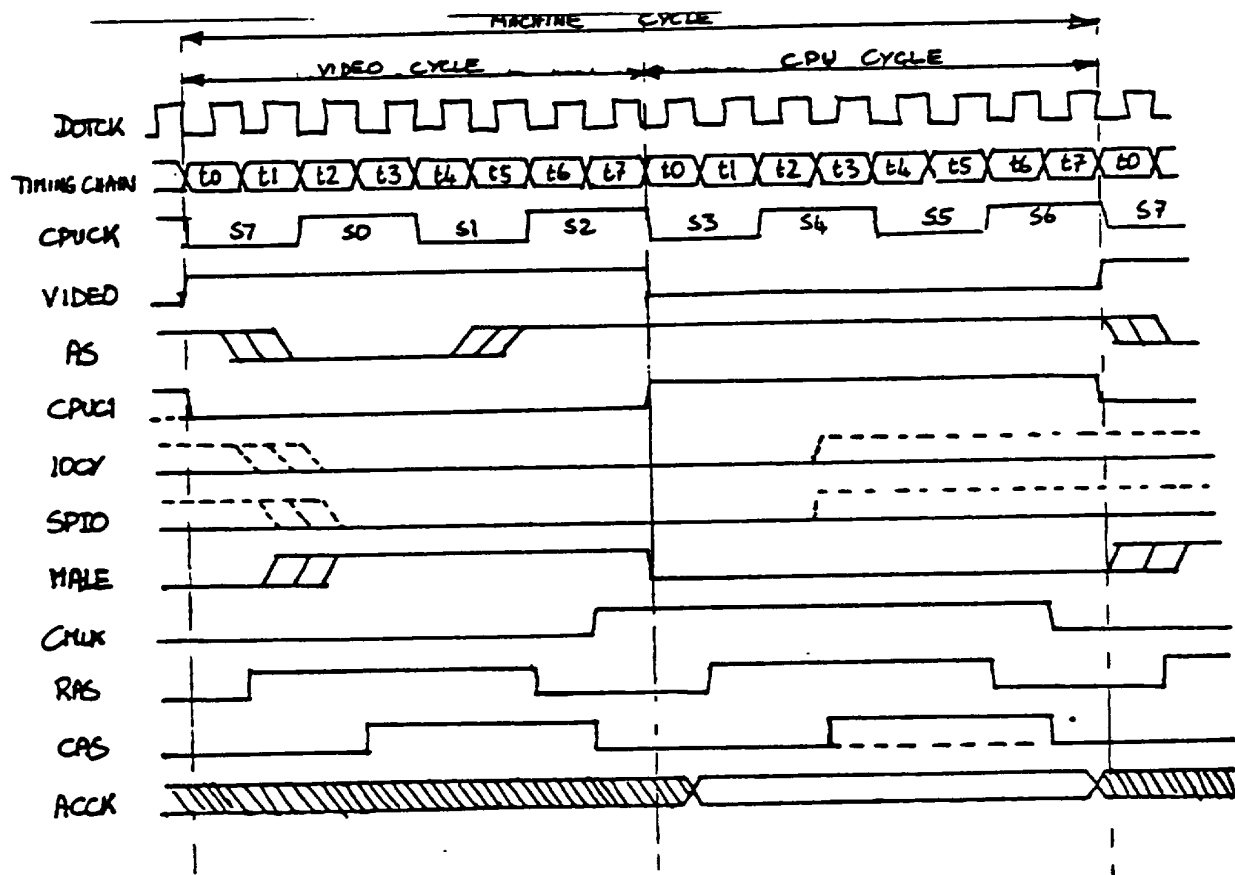
Figure 4-7. Processor Board Internal Timing

9b
4-13e

correspond, as shown in Figure 4-7.

This timing results in the address strobe (AS) signal being recognized during the video cycle, which permits the MMU to calculate and check the physical address in time for the result to be ready for the processor cycle.

The CPUC1 signal signifies the first cycle of a CPU instruction execution. The IOCY and SPIO signals indicate that an I/O or special I/O cycle is in progress. The IOCY and SPIO signals are generated from information contained in the MMU.

The Memory Address Latch Enable (MALE) signal is used as the selector between the two registers in the MMU that are associated with each logical address. When MALE is true, the segment origin register (SOR) is being accessed and the MMU is in the process of calculating the origin of the page being addressed. When MALE goes false, the segment limit register (SLR) is selected and the MMU calculates whether the address lies within the page limits.

The CMUX signal is used to select the source of the address which is to be presented to the memory. When deasserted, it gates the video address. When asserted, it gates the physical address presented by either the MMU or the DMA control.

Memory timing is controlled by the row and column address strobes (RAS) and (CAS). These and all of the other signals listed above are generated with reference to one or more of the t$\emptyset$ through t7 time periods.

4.2.2 Memory Management Timing

A logical address is being output from the 68$\emptyset\emptyset\emptyset$ when the address strobe signal is asserted. The MMU must process this and present the result to the memory on the basis of the type of access. In the case of a memory cycle, the physical address must be stable in time for presentation to the memory along with the row and column strobes.

In addition, the timing of each special I/O cycle with which data are written into an MMU register involves signals not used in any other operation. Figure 4-8 shows a sequence of operations as follows:

* The beginning of a relocate/check cycle
* The execution of a write to the MMU.

Figure 4-8. MMU Timing Diagram

The MALE signal selects between relocate mode, based
on the SOR, and check mode, based on the SLR. MALE
directly generates the base/limit (B/L/) selection
signal.

The FC2 signal originates in the 68000. It is
asserted to indicate that the processor is currently
in supervisor mode. Mapping is forced to the
supervisor context, context 0, when FC2 is
asserted.

A write cycle to the MMU is a special I/O cycle and
begins with the assertion of the SPIO signal, which
directly generates the MMUIO signal. This causes

Figure 4-8. MMU Timing Diagram

4-15
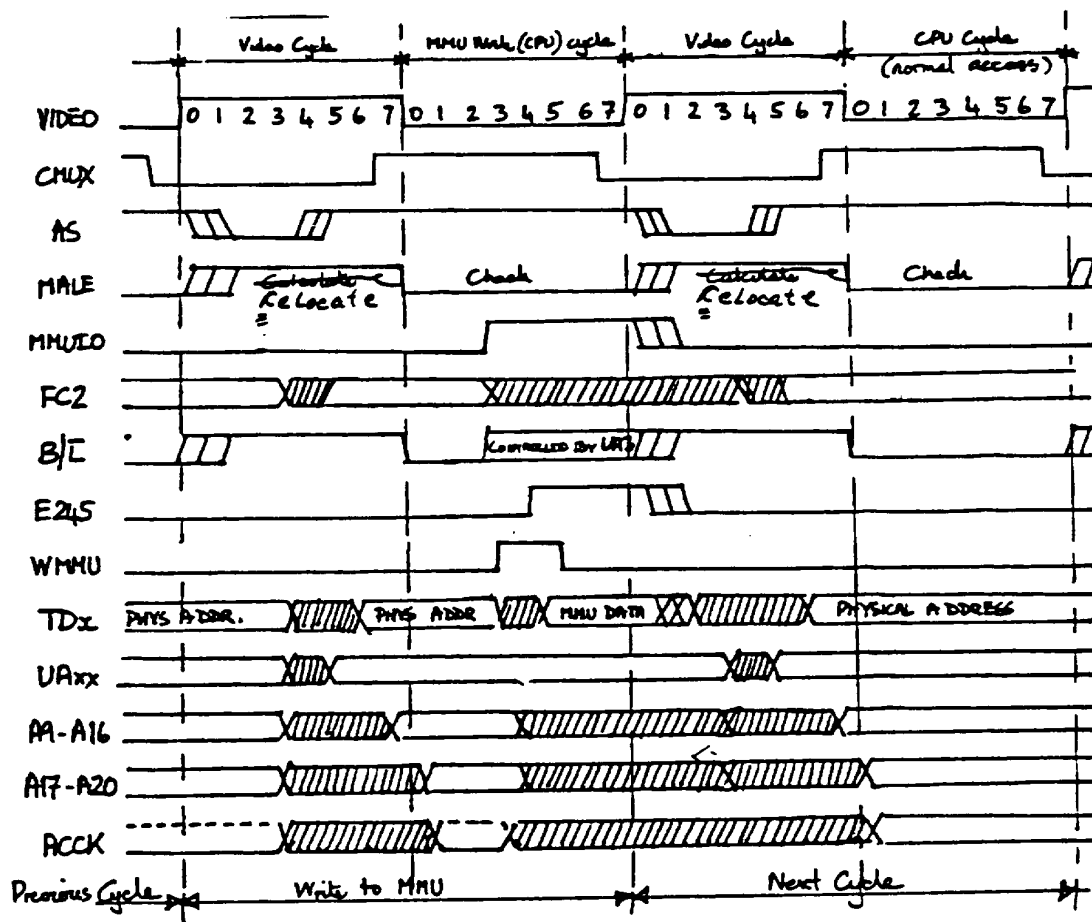
the B/L/ signal to be controlled by the UA3 address
line to select between the SOR and the SLR, and the
SEG1 and SEG2 bits define the currently addressed
context.

The output of the MMU memory is disabled when the
WMMU signal is asserted and the data to be written
is placed on the TD lines by means of the E245
signal.

Note that the address lines are divided into three
groups as regards timing. These are:

  * The unbuffered address (UA) lines. These
    do not pass through the MMU and are
    therefore stable first.

  * The A9-A16 lines. These are generated by
    the MMU and presented almost directly to
    the I/O decode and memory after the skew
    inherent in the MMU access time.

  * The A17-A2Ø lines. These suffer an
    additional delay due in the adder chain.

4.2.3 Memory Timing

The memory boards contain the memory array itself,
some error-detection circuitry, and the necessary
latches and drivers. Most of the memory control
signals are generated by the processor board and
presented to the memory board via the memory bus.

The 8ØØ ns 68ØØØ bus cycle includes two separate 4ØØ
ns memory cycles. The signals that control these on
the interface to the memory boards are shown in
Figure 4-9.

Figure 4-9. Memory Control Timing Diagram

The CMUX signal is used to select between the video
and the processor addresses being presented to the
memory. The contents of the RAx signals are
controlled by the CMUX and the RAS signals.

The A9-A16 and A17-A20 are generated by the MMU and
are used to generate column address and board or
device selection within memory. The RAS signal is
present for every video cycle unless the cycle and
once during every 68000 bus cycle.

The CAS signal is generated for each video cycle,
but can be absent from a processor cycle if no
memory access is taking place. This is indicated by
the deassertion of CASEN.

The VA8-11 are representative of the timing of all
video address signals. These are also used in the
generation of the refresh address in the memory
since video accesses are always to sequential
locations. Refresh takes place during the video
cycle.

Selection of refresh for a particular board is

September 1982
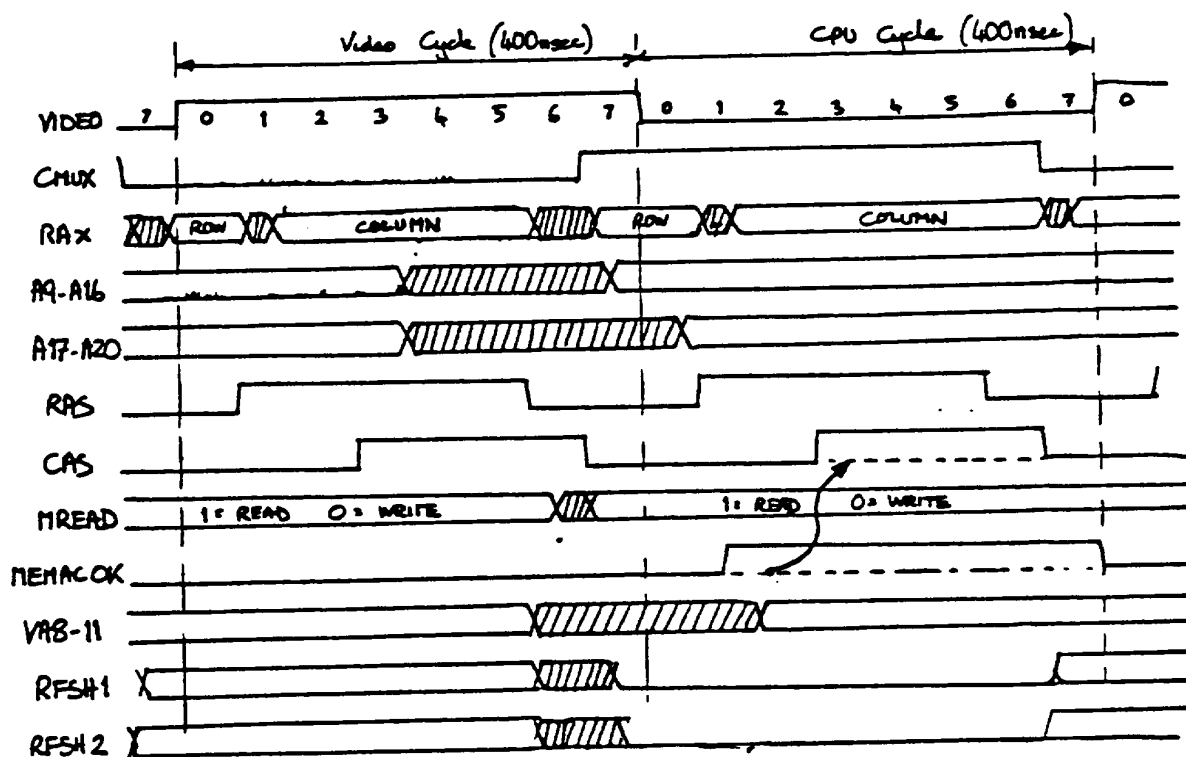
Figure 4-9. Memory Control Timing Diagram

4-17e

controlled by the RFSH1 and RFSH2 signals. Details
are discussed in section 5.3.

4.2.4 Video Timing

The video board, which contains the analog circuits
necessary to control the CRT, is described in
Chapter 8. Timing signals for the transfer of data
to the CRT are shown under processor board control.
Figure 4-10 shows the timing diagram for the signals
generated.

Figure 4-10. Video Control Timing Diagram

The video control contains a shift register that is
loaded at the end of a video access and then shifted
out at a rate of 1bit/50 ns, 20 MHz, to provide the
bit-serial data stream to the video board.

The data stream continues to be read whenever the
end of a line is reached and a horizontal retrace is
being performed. However, the data are ignored and
the video address counter is not incremented. In a
similar fashion, data are not read out during the
vertical retrace.
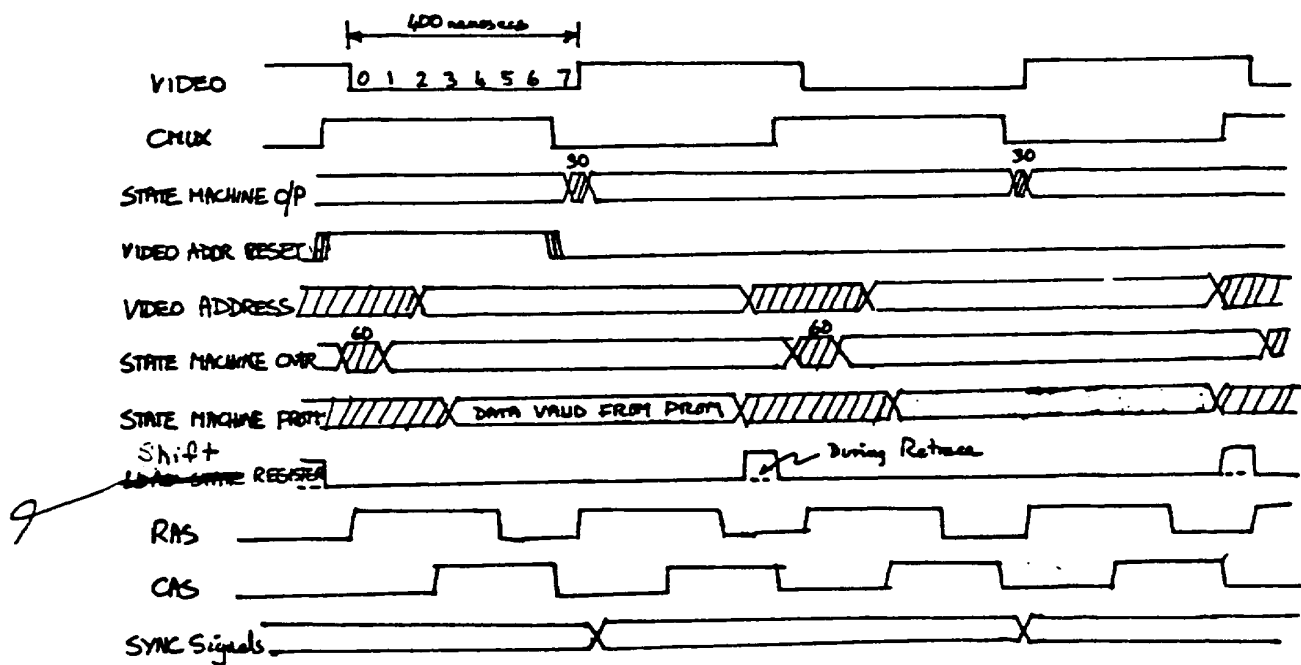
Figure 4-10. Video Control Timing Diagram

Timing for video control is performed by a state
machine and is synchronized with the VIDEO signal.
The shifting of the bits out to the video board is
performed by the DOTCK.

The state machine counter is clocked with the
falling edge of the VIDEO signal. The rising edge
of this signal latches the current output from the
state machine PROM.

The video address is reset once per page. This
occurs after 379 lines of 72Ø pixels each. Only 364
lines are displayed on the screen. The timing of
the video data within a page is shown in Figure
4-11.

Figure 4-11. Video Page Timing

The last pixel of each page must be a 1 (one) in
order that the retrace is black. This is done by
having a "one" in the least significant bit of the
32,767th byte displayed.

4.3 The Central Processing Unit

The heart of the Lisa is the 68ØØØ 32/16-bit processor,
which is described in detail in the 68ØØØ User's

Figure 4-11. Video Page Timing

4-21
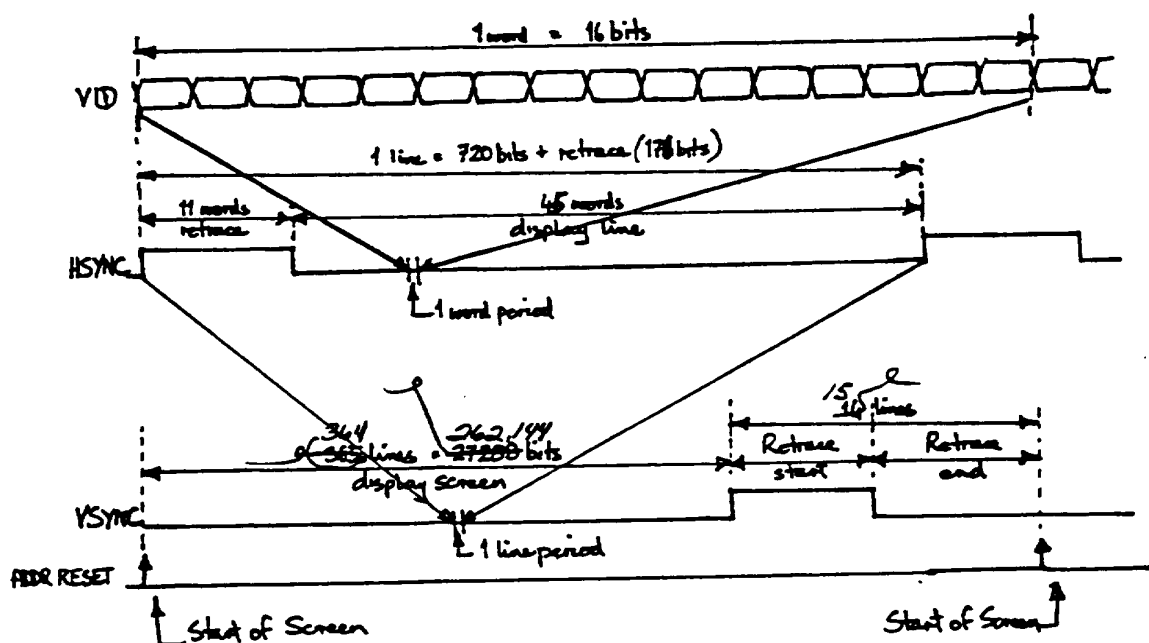
Manual. Refer to drawing Ø5Ø-4ØØ9 in Appendix A for
schematics of the devices discussed in this section.
Page 3 of the schematics shows the CPU at location
A3-D3.

4.3.1 Clock Generation

Timing generation is shown on sheet 2. At B-4,
crystal Y1 and its associated oscillator circuit are
used to generate the DOTCK and CK signals. These
both have a period of 5Ø ns and have the waveform
shown on Figure 4-12.

The DOTCK signal is used to provide timing to the
video control, which shifts bits serially to the
video board. These bits are then displayed on the
screen. CK drives the 4-bit synchronous counter at
D4, sheet 2, whose outputs are decoded to provide
the eight timing states tØ/ through t7/, plus the
VIDEO signal, as shown in Figure 4-12.

The QB output has a period of 2ØØ ns. It is used as
the 68ØØØ clock and also generates the main clock
CPUCK, which is distributed through the Lisa.

Figure 4-12. Processor Board Timing Generation

September 7th 1982
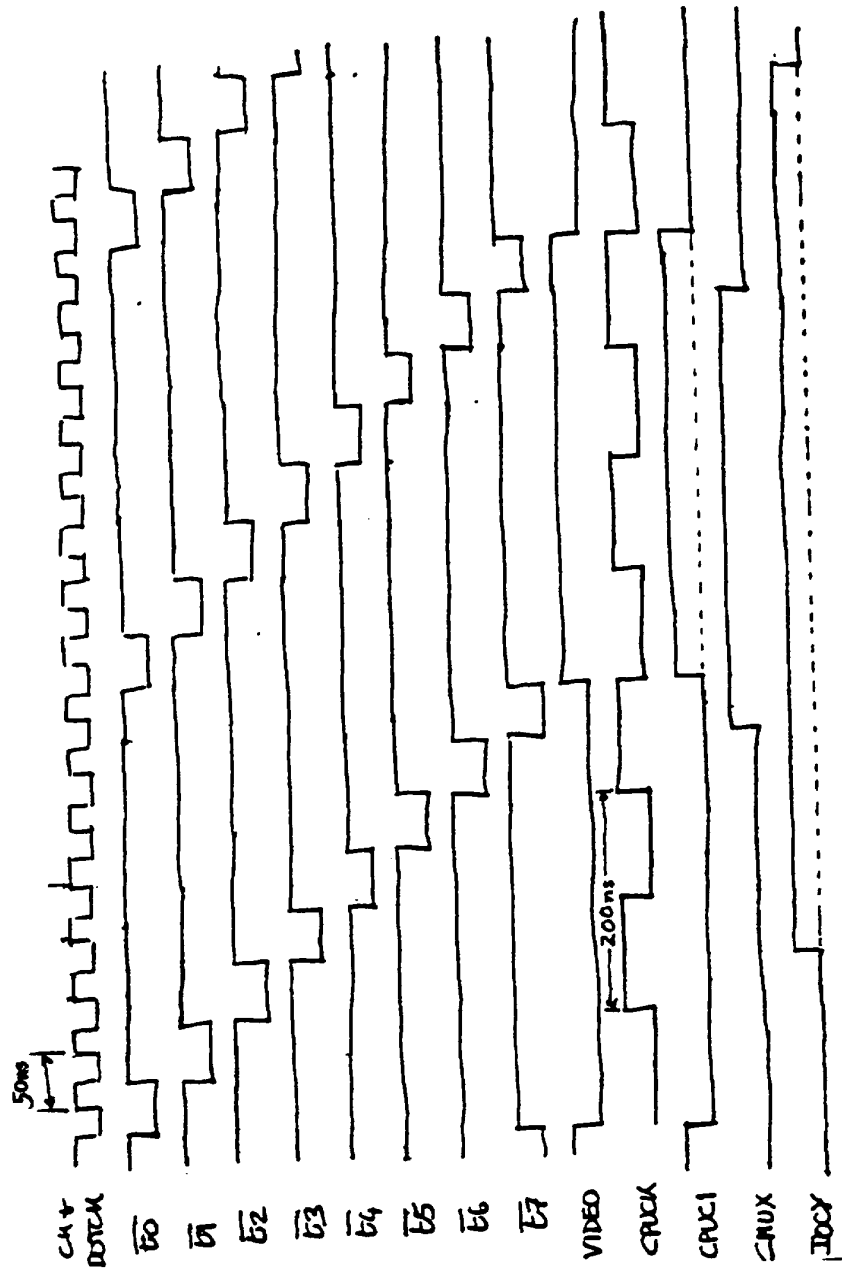
LISA Hardware Manual

Figure 4-12. Processor Board Timing Generation

4-22

4.3.2 Processor Control Signals

The six main bus control signals are buffered by the
LS244 at C-3 on sheet 3. This is enabled when the
bus grant acknowledge (BGACK/) signal has been
deasserted. In other words, the bus is released at
the same time that the bus grant acknowledge is
generated, which allows the device to take control
of the bus.

Note that UAS/ constitutes an unbuffered address
strobe, which is not gated as above. The 68000 is
synchronized with the AS signal. This signal should
be used for synchronization on the board whether the
bus is under CPU control or not.

The status signals FC0, FC1, and FC2 are decoded to
provide the IAK and IAK/ signals. These latter
signals are used to gate the address of the device
that generated an interrupt. The FC2 signal is used
to distinguish between supervisor and user mode
cycles.

Incoming interrupts are encoded by priority through
the LS148 at C-4 and presented to the IPL0-IPL2
inputs of the 68000. The system RESET is buffered
and chained through the 7417 at D-3, whose output is
pulled up through R12. Other control signals
interface directly to the bus drivers, with no
buffering.

4.3.3 Address and Data Lines

Address lines UA9 to UA23 are presented directly to
the MMU, since these are the bits that define the
segment and page of memory that is being addressed.
Refer to section 2.3 for a discussion of the MMU
address translation process.

The eight low-order bits, A1 to A8, are buffered
through the LS244 at A-3, sheet 3, which is gated
with BGACK/ to release the memory bus when the CPU
relinquishes bus control.

The 16 data lines, D0 to D15, are buffered by the
bidirectional LS245s at A-4 and B-4. These are
enabled by the DBON/ . The direction is selected by
the READ signal.

4.3.4 Bootstrap ROM

The bootstrap ROM is used during power-up to provide
initial programs that permit the operating system to
be loaded from a mass storage peripheral, and the
Lisa itself, to be initialized to a known
configuration.

The ROM is accessed by means of special I/O cycles.
The ROM consists of the two devices shown at
locations A-2 and B-2 on sheet 3.

Note that the ROM is addressed directly by the
address lines from the 68000. This means that the
ROM addressing does not require that the MMU be
operational. Therefore bootstrap routines execute
correctly out of ROM before the MMU has been
configured at initialization time.

The ROM is enabled by the ROM/ signal. This signal
is asserted whenever a special I/O cycle is in
process while UA15 is high and UA16 is low.

4.4   The Memory Management Unit (MMU)

The function of the MMU is to translate logical
addresses used by the software into physical addresses.
This is performed in terms of logical pages of 512 bytes
within logical segments of 128 Kbytes.

The operation of the MMU is discussed in section 2.3
above. Address lines UA1-UA8 are not operated on by the
MMU. UA17-UA23 are used to select one of the 128
possible logical segments, while UA9-UA16 address a page
within that segment.

At the same time, the entire logical address space is in
one of four possible contexts, selected by the SEG1 and
SEG2 signals. The MMU has four identical sets of
registers, one for each context of 128 segments.

Each segment has two registers associated with it. The
SOR contains 12 bits that give the page number with that
the segment begins. The SLR contains 8 bits that supply
the number of physical pages assigned to this segment,
plus 4 bits that indicate the physical address space and
other data about the physical segement.

The MMU is shown in simplified form in Figure 4-13. It
is used to define three distinct physical address
spaces. This is discussed in Chapter 2 in some detail.
Refer also to Figure 2-4. The 68000 can access a
maximum of 2 Mbytes of RAM, which is located on up to
two boards, plus a distinct I/O space and an additional

special I/O space. Each address space is a 2 Mbyte
block.

The MMU logic is shown on sheet 4 of schematic 050-4009
in Appendix A. It consists of RAM storage for the
segment registers, address latches, and logic that
permits the contents of the registers to be
manipulated.

Figure 4-13. MMU Block Diagram

Figure 4-13. MMU Block Diagram

4.4.1 MMU RAM Storage

The registers of the MMU are organized within a 1K
by 12 bit RAM memory matrix. These can be altered
by software when the 68000 is in any mode. The
operating system is responsible for controlling
access to these registers. The register addresses
are generated from the logical address. Their
contents define the physical address.

The Lisa has a 16 Mbyte logical address space
because of the architecture of the 68000. This
entire space can function in one of four contexts,
depending on the configuration of the SEG lines.

Each 16 Mbyte space is divided logically into 128
segments, each of which is allocated a pair of
registers in the MMU that define segment
parameters. This results in a total of 1024
registers, since the four contexts each contain 128
segments and each segment requires a pair of
registers. This is shown in Figure 4-14.

```
        -----------------------------------
           Segment Ø Base  (SOR)      ^
           Segment Ø Limit (SLR)      |
                                      |
           Segment 1 Base             |
           Segment 1 Limit            |
                                      |
           Segment 2 Base             |
           Segment 2 Limit            |
                  .             Context Ø
                  .                   |
              128 pairs total         |
                  .                   |
                  .                   |
           Segment 127 Base           |
           Segment 127 Limit          v
        -----------------------------------
           Segment Ø Base             ^
           Segment Ø Limit            |
                  .                   |
                  .                   |
              128 pairs total   Context 1
                  .                   |
                  .                   |
           Segment 127 Base           |
           Segment 127 Limit          v
        -----------------------------------
           Segment Ø Base             ^
                  .                   |
                  .                   |
              128 pairs total   Context 2
                  .                   |
                  .                   |
           Segment 127 Limit          v
        -----------------------------------
           Segment Ø Base             ^
                  .                   |
                  .                   |
              128 pairs total   Context 3
                  .                   |
                  .                   |
           Segment 127 Limit          v
        -----------------------------------
```
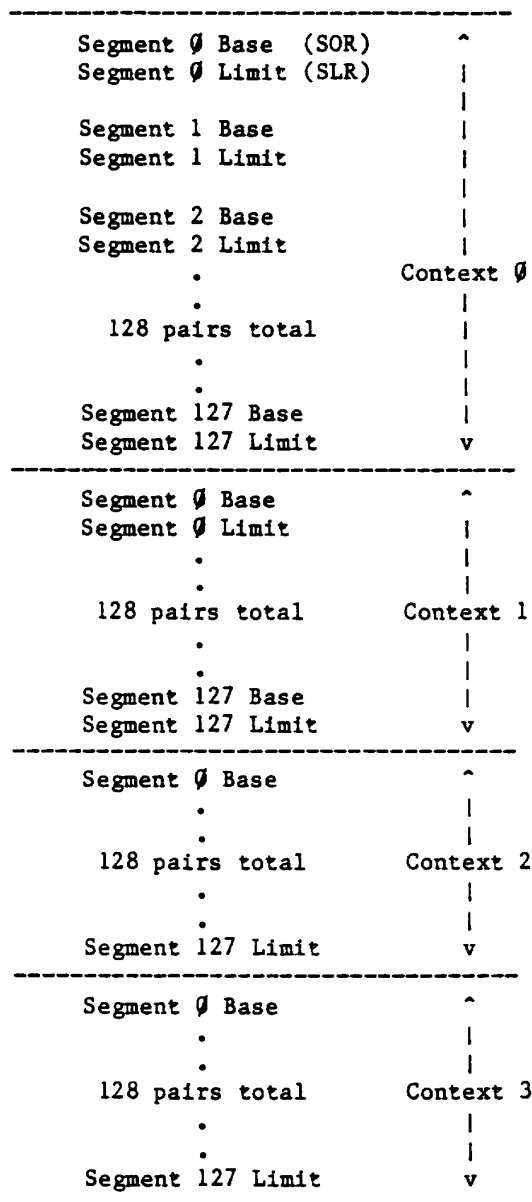
Figure 4-14. MMU Memory Configuration

The two registers for each segment are known as the
SOR and the SLR, as described in Chapter 2.

The SOR defines the physical address of the first

byte of the segment. This is given as a multiple of
512-byte blocks. The first block in memory is thus
defined by address ∅∅∅∅∅∅@16.

The SLR defines the size of the segment in terms of
multiples of 512-byte pages. It also contains a
4-bit code that defines the type of space, as
outlined in Figure 2-4.

The MMU memory is thus logically divided into four
sets of 128 pairs of 12-bit registers, each set
being used only when the 68∅∅∅ is running in the
corresponding context. This enables software to
perform context switching very rapidly.

Referring to schematic ∅5∅-4∅∅9, page 4, the ten
lines used to address the MMU RAM can be seen as
consisting of the following:

  * UA17-UA23, 7 address lines,
  * MS1 & MS2, from SEG1 & SEG2 lines,
  * B/L/ , the base/limit select.

The address lines are the unbuffered high-order
address lines from the 68∅∅∅ CPU on sheet 3. The
other signals are generated in the logic at C-4.
Refer to Figure 4-8 for the timing relationships.

The crucial element of operation in the MMU is that
it must first generate the physical address that is
the origin of the memory page to be accessed. Then
it must check whether the address lies within the
limits of the page addressed.

These two functions are selected by the memory
address latch enable (MALE) signal, which originates
in a S1∅9 JK flop on sheet 2. MALE is asserted at
the end of a CPU cycle when the AS signal becomes
deasserted. This typically occurs around the t3
period of the video cycle. This asserts the B/L/
signal through the LS∅∅ gate at C4, on sheet 4,
which selects the base register.

The SEG1 and SEG2 latch is shown on sheet 5. The
software defines the context in which the CPU is
currently running by means of these two signals,
except if the CPU is running in supervisor mode.
Supervisor mode is indicated by the FC2 signal being
asserted. The segment being addressed is defined by
the UA17-UA23 signals.

When the conditions exist to set the CPUC1 JK flop
at B-2 on sheet 2, the same term is used to reset

the MALE flop at A-2. This occurs at the end of t7
time during the video cycle. With MALE deasserted,
the B/L/ term also becomes deasserted and the SLR
that corresponds to the SOR just accessed is used to
check the access limits and also give the type of
cycle to be performed.

4.4.2 SOR and SLR Initialization

The MMU registers are in an undefined state when the
Lisa is first powered on. The bootstrap ROM is not
addressed via the MMU. This enables the CPU to
operate initially without requiring that the MMU be
functional.

Before RAM can be used, the registers that
correspond to the contexts and segments being used
must be initialized. The RAM that is used as the
MMU register storage is accessed via special I/O
space. This is decoded by the LS139 device at D-2
on sheet 5. The MMUIO/ signal enables the WMMU/
signal via the JK flop at D-4, on sheet 4. Refer to
Figure 4-9 for signal timing relationships.

Each register is written to in a separate write
cycle. The SEG1 and SEG2 lines are configured to
the appropriate context and the UA17-UA23 lines
select the segment. When the registers are written,
the SOR or SLR are selected by the state of the UA3
line through the LS$\emptyset\emptyset$ gate at C-4 on sheet 4.

The MMUIO signal is asserted when all the following
conditions exist:

1. The SPIO signal is asserted
2. UA15 is asserted
3. UA16 is deasserted.

When MMUIO becomes asserted, the clear input of both
S1$\emptyset$9 JK flops at D-4 are released, allowing the E245
signal to be asserted at t4 time and WMMU/ to be
deasserted at t3 time if the 68$\emptyset\emptyset\emptyset$ is performing a
read cycle.

The data to be written into the registers is
presented to the MMU RAM via the two LS245
bidirectional drivers at C-3 and D-3. The direction
in which the data are moved is controlled by the
READ signal from the CPU.

The TD lines from the lower LS245 write the two
low-order nibbles into the lower RAMs. The upper

nibble is base data for the SOR or access-type data
for the SLR. Register contents can be read via the
same path.

4.4.3 Address Translation

During the video half of the 68000 bus cycle, the
SOR contents are read out as a 12-bit physical
address that defines the physical address of the
beginning of the segment at a 512-byte boundary.

This value is added to the page address that is
presented to the other inputs of the adder by
UA9-UA16. Note that the high-order input nibble is
forced to zero. The result is presented to the
LS373 latch at C-2 and the LS374 latch at B-2. On
the falling edge of the MALE signal, which occurs at
the end of the calculation involving SOR, the
physical address is latched. This will be stable on
the A9-A20 lines if the BGACK/ signal is deasserted,
no DMA access in process, and CMUX is asserted to
avoid conflict with the video address.

MALE being deasserted signals the second half of the
68000 bus cycle, when the access limits are
checked. The B/L/ signal changes polarity and the
contents of the SLR are read out.

The eight low-order bits, which indicate the number
of pages contained in this segment, are also added
to the page address given by the UA9-UA16 lines from
the CPU. The overflow line from the second nibble
is the access check (ACCK) signal. If ACCK is
asserted, this indicates that the desired page lies
outside the limit set for the segment in question.

An exception to this occurs when the control bits
indicate that the accessed segment is a stack
segment. Since the stack begins at the high-order
address within the block, the significance of ACCK
is inverted in this case. This function is
implemented in the S86 gate at B-3 on sheet 2.

An overflow results in the suppression of the CAS/
signal, which prevents any memory operation from
taking place. The output of the high-order nibble
of the adder is ignored.

The high-order nibble of the SLR contents provide
flags for the type of segment that is being
accessed. These indicate:

* Segment in memory space (MEM)

* Segment in I/O space (IO)
* Segment that is read-only (RO)
* Segment that contains the stack (STK).

Refer to Figure 2-4 for the full coding permutations possible, since all combinations are neither valid nor covered by the above. These signals in turn generate the appropriate control signals for the type of segment indicated.

The MEM term being asserted, MEM/ low, enables the CAS signal for a memory access via the LS$\emptyset$2 gate at C-3 on sheet 2.

The IO term being asserted initiates an I/O cycle via the IOCY flop at B-1 on sheet 2.

The RO term being asserted inhibits a write cycle to memory via the ALS32 gate at B-3 on sheet 2. It also inhibits an SPIO cycle by being one of the terms on the LS26$\emptyset$ gate at C-1.

The STK term being asserted causes a carry input to be presented to the low-order adder via the F$\emptyset$2 gate at A-3 on sheet 4. This is done because of the stack configuration, which begins at the top of the segment and decrements through memory from there.

4.4.4 Memory Timing Generation

Memory control timing is shown in Figure 4-9. Since the nine low-order bits of the address are presented directly from the CPU, these are used as memory row addresses. This avoids the need to wait for the output of the MMU to become stable before any memory addressing can be done.

The RAS is enabled through the LS32 OR gate at D-4 on sheet 2 of the schematics. RAS goes true at the end of the t$\emptyset$ state and goes false at the end of t5. Note that RAS is generated even for cycles that turn out to be I/O or erroneous. This does no harm provided that CAS is generated for such cycles. The only time that RAS is generated for a memory cycle is if the current cycle is a video cycle and is not the first of a multi-cycle CPU access.

The CAS has an enable signal that is the logical OR of a number of terms:

  * If a video cycle is in process

         * If a DMA cycle is in process (BGACK!.CPUC1)
         * If no error was detected in a memory
           cycle.

    This last term requires that a number of factors be
    satisfied:

      * A memory cycle is in process (MEM!.CPUC1),
      * No attempt is made to write to a read-only
        segment (READ/!.RO),
      * The segment limit was not exceeded (ACCK).

    If CAS is enabled, it will go true at the end of t2
    and goes false at the end of t6.

    The signal requesting a read from the memory is
    MREAD. It is generated through the S$\emptyset$2 gate at D-2
    on sheet 5. Refresh of the memory is generated by
    two gates at A-4, sheet 2. One of the two signals
    R1 and R2 is provided to the memory board for use as
    a refresh enable. Each occurs when either, but not
    both, of the VA8 and VA11 video address signals is
    asserted.

4.5   Video Control

    The video control is shown in Figure 4-15 and consists
    of the following components:

      * Video address counter, VA1-VA14,
      * Shift register
      * Video state machine
      * Video page register, VA15-VA2$\emptyset$.

    The 32 Kbytes of memory in which a full video screen is
    stored is sequentially accessed once every 1/6$\emptyset$th of a
    second.

Figure 4-15. Video Control Block Diagram

4.5.1 Video Address Counter

The video address counter points to the location in
the 32 Kbyte video page of the next data byte to be
fed to the display. It is incremented once for
every 16 active pixels that are fed into the video
board, and it is reset at the end of each vertical
retrace.

The circuitry is shown on sheet 5 of schematic
Ø5Ø-4ØØ9. It consists of the two LS393 counters at
B-4. The counters are arranged in series and the
outputs fed to the memory address MUX in the upper
right of sheet 4. The counter is clocked on the
leading edge of each t7 state via the JK flop at
B-3, sheet 5. It is reset synchronously with CMUX
when the video state machine determines that the
vertical retrace has been completed.

4.5.2 Video Data Shift Register

This is used to convert the 16-bit words of video
data read out of memory into the serial data stream
required by the video board.

The circuit is also shown on sheet 5 of the
schematics. It consists of the two LS166 devices at
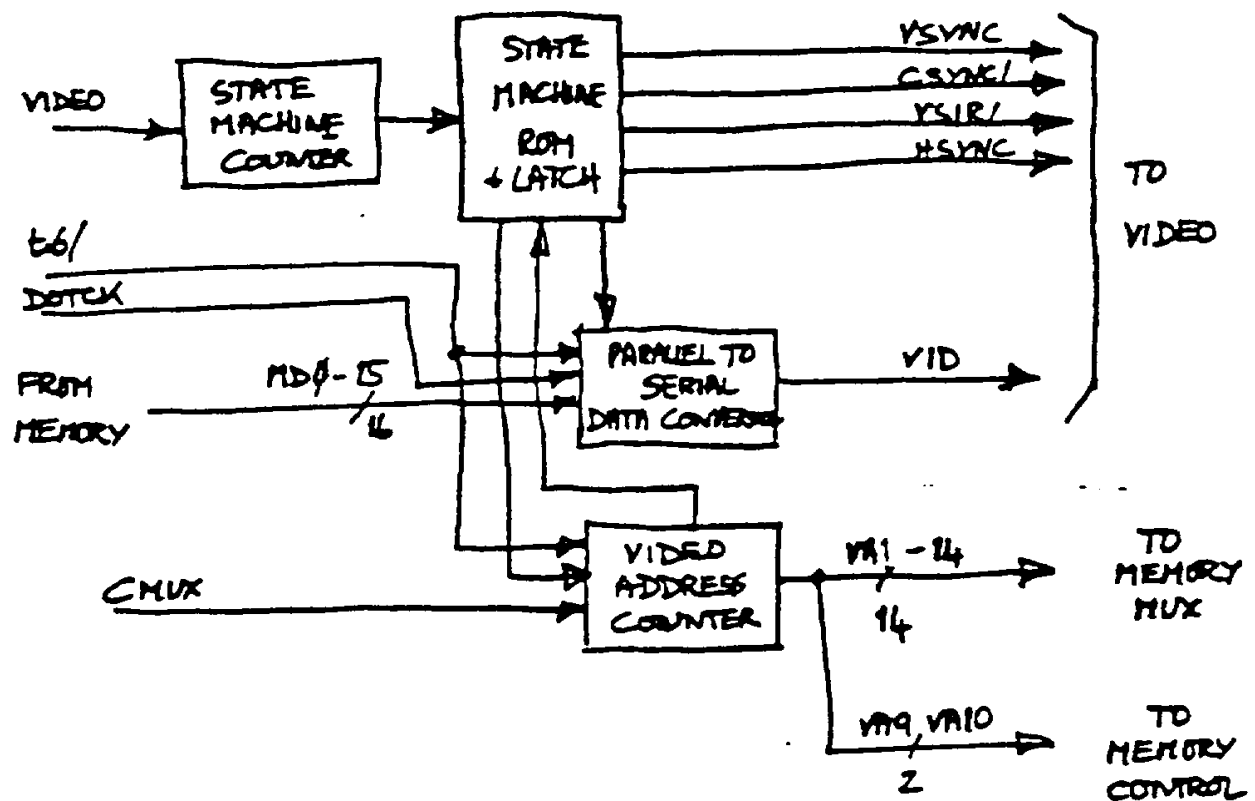
Figure 4-15. Video Control Block Diagram

27b
4-34c

B-3 and some associated circuitry. The clock that
increments the video address counter is also used to
parallel load the shift register with data presented
on MDØ-MD15.

The DOTCK signal from C-4 on sheet 2 is used to
shift the data out to the VID output via the JK flop
at C-3 on sheet 5. This flop has been inserted in
the data path to ensure a uniform hold length for
each data bit. If this were not present, the final
bit in each word could be curtailed, since the next
word is parallel-loaded into the shift register.

The INVID/ signal provides an inverted polarity of
the video signal. It can also be used as a serial
input to the shift register for test purposes. The
shift register presents a pixel to the video board
every 5Ø ns.

4.5.3 Video State Machine

The video state machine is used to monitor the
position on the screen at which the current data are
to be placed. It counts up to the number of words
in one line, performs a horizontal retrace, resets
itself and then resumes. At the bottom of the
screen it performs a vertical retrace.

The machine is shown on sheet 5 of the schematics
and consists of the LS393 counter at D-4, the 63Ø9-1
programmable ROM (PROM) at D-4, and the LS374 latch
at D-3. The counter is clocked with the video
signal. The video does access memory during the
video retrace periods. Both the counter outputs and
the VA9 and VA15 signals are used to address the
PROM. The data output from the PROM is latched in
the LS374 with the opposite edge of the same signal
that clocks the counter.

The HSYNC/ and VSYNC/ signals are presented to the
video board for use in horizontal and vertical
synchronization of the data on the screen. Other
outputs are used to clear the video address counter
at the end of vertical retrace, generate the VSIR/
to interrupt the CPU during vertical retrace for
cursor positioning and reset the shift register
load flop and the state machine counter itself.

The state machine performs 45 normal word fetches
and shifts in each line before performing a
horizontal retrace and resetting itself. When it
detects the 364th line by monitoring VA15, it
generates a vertical sync of 6 lines duration,

followed by vertical sync termination of an
additional 9 lines duration.

4.5.4 Video Page Register

The Video Page Register contains the six high-order
bits of the address to be presented to memory, which
are not provided by the Video Address Counter
(A15-A2Ø). This provides a physical address to the
memory, that is, it is not translated by the MMU.

The circuit consists of the LS374 at Bl on sheet 4.
It is loaded by the VAL/ signal, which is decoded
from an I/O command at B-2 on sheet 5. It is gated
as an address whenever the CMUX signal is false.

4.6   Bus Interfaces

The processor board interfaces to three other components
inside the cabinet. These are the:

  * System bus
  * Memory board(s)
  * Video board.

The bus interfaces to all three are made by a single
connector to the motherboard and are shown schematically
in Figure 4-16.

The system bus on the motherboard is extended in part to
become the expansion bus. This bus is effectively a
subset of the system bus used by the I/O board. It is
described in detail in section 3.4 of this manual.

Figure 4-16. Processor Board Bus Interfaces

4.6.1 System Bus Interface

   The system bus operates under control of the
   processor board during most normal operations. An
   exception occurs when a peripheral controller
   performs data transfer to or from memory by means of
   a DMA operation.

   Refer to Figure 4-16 for a signal list and pin
   assignment. An overview is also shown on sheet 1 of
   schematic 050-4009.

   The system bus interface signals can be divided into
   the following categories:

     * Address lines
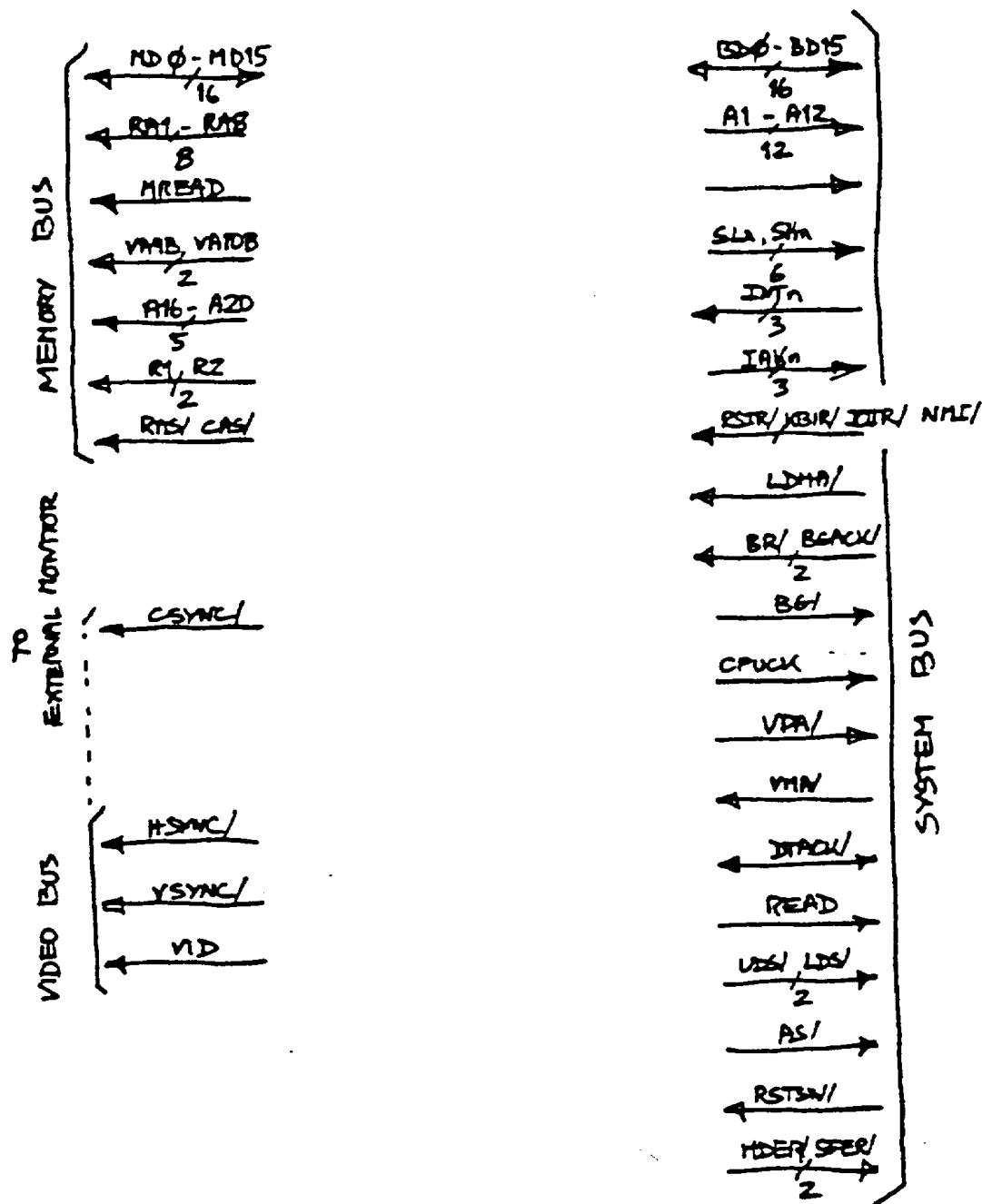
Figure 4-16.   Processor Board Bus Interfaces

* Data lines
* Asynchronous control lines
* Bus arbitration lines
* Interrupt control lines
* Processor board control lines
* I/O slot enable lines.

Address Lines

These consist of the 12 lines, A1 through A12,
that are used to provide a physical address on the
bus. A1 through A8 originate in the LS244 at A-3
on sheet 3, while A9 through A12 come from the MMU
output latches at A-2 and B-2 on sheet 4. All
signals to the bus are disabled by the BGACK/
signal being asserted.

Data Lines

These consist of the 16 lines, BD0 through BD16,
that are used to transfer data on the bus. All 16
lines originate in the LS245 bidirectional drivers
of both the CPU and the memory matrix at A-4 and
B-4 on sheet 3. The CPU lines are enabled by the
DBON/ signal, which is generated at B-2 on sheet 5
by having both the BGACK/ and SPIO/ signals
deasserted. The memory lines are enabled by the
MDEN/ signal which is synchronous with the CPUC1
signal whenever both IOCY/ and SPIO/ are false.
This is shown at A-4 of sheet 3.

Asynchronous Control Lines

The following are used to control data transfers
made on the bus.

AS/ strobes: a valid address that is
present on the A1-A12 lines. It originates
at C-3 on sheet 3.

READ: defines the cycle to be from memory
to the accessing peripheral or processor.
It originates at C-3 on sheet 3.

UDS/ and LDS/ : the upper and lower data
strobes that define on which half of the
BD0-BD15 lines a byte transfer is being
made. They originate at C-3 on sheet 3.

DTACK/ : a data transfer acknowledge that
indicates to the current bus master that

the asynchronous operation has been
completed.

CPUCK: the clock used for the CPU itself.
It is presented on the bus for
synchronization purposes.

Bus Arbitration Lines

These signals are used to determine which device
can operate as a bus master.

BR/ : the bus request line that is asserted
by a slave device that wishes to have
control of the bus.

BG/ : the grant signal with which the
current master allows the requesting slave
to take control of the bus. The signal
originates directly on the CPU at C-3 on
sheet 3.

BGACK/ : the signal with which the slave
acknowledges that it has accepted the bus
grant and has taken control of the bus.

Interrupt Control Lines

The following are used to determine the source of
an interrupt and to acknowledge that the interrupt
is being processed.

NMI/, RSIR/, INT0/, INT1/, INT2/, KBIR/,
and IOIR/: signals presented to the
processor board as an interrupt request.

IAK0/-IAK2/ : the coded responses to an
interrupt request that indicates which
requesting device is being serviced.

Processor Board Control Lines

These signals are used for general control and
information within the Lisa.

RESET/ : a signal to the Lisa to return to
its original on state.

LDMA/ : the signal to load the upper DMA
address latch, which is located at D-1 on
sheet 3 of the schematics. This signal

originates in the peripheral performing the
DMA which needs to have the DMA upper
address altered.

E: the enable signal for use with 6800-type
peripheral devices.

VPA/ : an indication that a 6800-type
peripheral is attached to the bus and has
been addressed.

VMA/ : the response of the CPU to a VPA/
signal and notifies the peripheral that a
valid address is present on the bus.

Slot Enable Lines

These lines decode the addresses of I/O slots that
are not present on the processor board. They are
presented to the bus as enable signals.

SL0/ -SL2/ : indicate that a slot low
decode has been made for an I/O transfer to
or from one of the three possible expansion
boards. The signals originate in the
decode logic at B-2 on sheet 5.

SH0/ -SH2/ : indicate the same for a high
decode.

INTIO/ : indicates a decode of the
processor board I/O space.

4.6.2 Memory Bus Interface

The memory bus is used to provide control signals to
the memory boards installed in the Lisa and also to
perform transfers of data between the memory matrix
and the rest of the memory. The signals are located
on the same common connector to the motherboard as
the system bus interface.

The signals that compose the memory bus are
described below.

A16-A20: address lines used for internal
decoding within the memory matrix and between
installed memory boards. Refer to Chapter 5
for details.

RA1-RA8: the multiplexed address lines used
to address the dynamic RAM array in
conjunction with the RAS/ and CAS/ timing
signals.

MD0-MD15: the data lines across which a word
of data is transferred to and from the
memory array. They originate at A-4 to B-4
on sheet 3.

MREAD: the memory read signal that indicates
the direction of transfer. It is generated
from the coincidence of the CPUC1/ and READ
terms at D-2 on sheet 5.

RAS/ and CAS/ : the row and column strobes
that indicate the contents of the RA1-RA8
lines. They are generated at D-1 and C-1 on
sheet 2.

HDER/ : indicates a hard memory error, which
is an error found to be uncorrectable if any
Error Correction Code (ECC) is present in the
memory. It is received by B-2 on sheet 3.

SFER/ : indicates a soft memory error, which
is an error in memory that could be corrected
by any ECC present in the memory.

VA9B and VA10B : video address lines
presented to the memory board for use in row
refreshing.

R1 and R2 : signals that indicate which of
the two possible memory boards is to be
refreshed.

4.6.3 The Video Interface

The Video Interface also shares the main connector
to the motherboard and consists of the signal group
listed below.

HSYNC/ : the horizontal sychronization pulse
used to indicate to the video circuit that
the end of a line has been reached. It
originates in the output of the video state
machine and is shown at C-3 on sheet 5.

VSYNC/ : the vertical sychronization pulse
used to indicate to the video board that the
bottom of the screen has been reached. It
originates in the video state machine at C-3

on sheet 5.

CSYNC/ : a composite of the above two signals
and is used as an output to an external video
monitor. It originates in the video state
machine at C-3 on sheet 5.

VID : the data bit-stream output to the video
board. It originates at C-3 on sheet 5.

4.7 Decode and Latches

This section includes the miscellaneous circuitry
present on the processor board but not included in the
preceding. It can be considered under the following
headings:

* I/O decode
* Processor board control register
* Memory error latch
* Processor board status latch
* Time delay logic.

4.7.1 I/O Decode

This is located at the extreme right of sheet 5 of
schematic Ø5Ø-4ØØ9. The first stage consists of the
LS138 1-of-8 decode device at A-2. This is enabled
when an I/O cycle is in process via the IOCY term
and the JK flop at A-2. The A16/ term must be
asserted.

The resulting decode of the A13-A15 terms results in
the eight decodes for the ranges shown. All but the
high-order decode are presented to the memory on the
system bus as described in subsection 4.6.1 above.
The final term is CPUIO/ , which is used to enable
the processor board I/O decode performed by the
LS139 decoder at B-2 on sheet 5.

The A11 and A12 terms are decoded to give the
address block decodes as follows:

RBES/ (F8ØØ-FFFF), the Read Bus Error Status,
which is used to gate the processor board
status latch at B-2 on sheet 3 onto the data
bus.

RMEA/ (FØØØ-F7FF), the Read Memory Error
Address signal, which gates the latched
address at D-1 and D-2 on sheet 3 onto the

data bus.

VAL/ (E8ØØ-EFFF), the Video Address Latch
signal, which is used to load the upper 6
bits of the video address (A15-A2Ø) at B-2
on sheet 4.

SYSC/ (EØØØ-E7FF), the Processor Board
Control Register signal, which is used to
load the LS259 latched decoder at D-2 on
sheet 5. Refer to subsection 4.7.2.

Decode during special I/O is done by the other half
of the LS139 at B-2. It is enabled by the SPIO/
term and decodes UA15 and UA16 to give the ROM/ or
MMUIO/ signals. These respectively enable the boot
ROM on sheet 3 and allow data in the MMU registers
to be modified or read.

4.7.2 Processor Board Control Register

The processor board control register is shown at D-2
on sheet 5. It is used to hold control signals used
internally on the board. It is loaded by the SYSC/
signal as described in the previous subsection. The
signals latched have the following functions:

DIAG1/ and DIAG2/ : used to force a soft and
a hard memory error respectively for
diagnostic purposes. They do this when a
write operation is performed to memory. This
can be seen by the gating terms at D-2 on
sheet 5.

SEG1 and SEG2: used by the software to select
the context in the MMU in which the address
translation takes place. They are input to
the MMU RAM addressing logic at C-4 on sheet
4. Functional details are discussed in
section 2.3.

START/ : used to disable the start mode. It
is used when the program is to execute out of
ROM after a power-on or reset. It enables
access to the MMU RAM via the LS32 gate at
B-4 on sheet 4.

SFMSK/ : used to suppress the detection of a
soft memory error. It is applied to the
LS279 Quad RS device at C-2 on sheet 3 to
inhibit detection of the SFER/ signal.

VTMSK/ : used to suppress the vertical
retrace interrupt to the CPU. It is input to
the interrupt latch at B-2 on sheet 3.

HDMSK/ : similar to SFMSK/ above but
suppresses the detection of a hard memory
error. It is input to the latch at B-2 on
sheet 3.

4.7.3 Memory Error Address Latch

When either a hard or a soft memory error occurs,
the processor board makes the address at which the
error occurred available to software.

The latch consists of two LS374 octal latches, shown
at D-1 and D-2 on sheet 3. The address is updated
each memory cycle by using the CAS signal from sheet
2 as the gating term to the LS11 gate at C-1, which
provides the clock to the latches. The occurrence
of either type of memory error prevents any updating
by blocking CAS at this gate. Resetting the error
latch permits normal operation again until the next
error occurs.

Note that only the 15 high-order memory lines
(A6-A2$\emptyset$) are latched, because this defines a 64-byte
block within memory, which is sufficient to locate
the physical page of memory causing the error. Lisa
software can map out faulty memory using the MMU in
pages as small as 512 bytes.

The low-order bit in the latch is not a memory
address bit. It indicates whether a CPU access or a
video access was in progress when the error
occurred.

For the case of a video error, only bits A15-A2$\emptyset$
contain valid information. Bits A6-A14 are
undefined.

4.7.4 Processor Board Status Latch

The processor board status latch is shown at B-1 on
sheet 3. It consists of an LS279 quad RS flop and
an LS244 octal driver. It is interrogated by the
RBES/ signal, which originates in the I/O decode
logic on sheet 5.

Four of the bits are latched by the LS279. These
are:

SFER/ , Soft Memory Error, which indicates a
recoverable error in memory. This can be
inhibited or reset by means of the SFMSK/
signal, in the processor board control
register at D-2 on sheet 5.

HDER/ , Hard Memory Error, which indicates an
unrecoverable error in memory. This can be
inhibited or reset by means of the HDMSK/
signal from the processor board control
register at D-2 on sheet 5.

VTIR/ , Vertical Retrace Interrupt, which
originates in the video state machine on
sheet 5. It can be inhibited by means of the
VTMSK/ signal from the control register on
sheet 5.

BUST/ , Bus Timeout Error, which originates
in the Time Delay Logic at D-4 on sheet 3.
This is reset by reading the Memory Error
Address latch, which generates the RMEA/
signal.

The other three bits available are not latched and
all originate in the video control logic on sheet
3. They are:

INVID, Inverted video, which can be
hand-wired to provide the inverse of the
video data normally presented to the video
board.

VID, Video Data, which is a direct sense of
the current bit stream being presented as
data to the video board.

CSYNC/ , Composite Synchronization pulse,
which originates in the video state machine
as a composite of horizontal and vertical
retrace signals.

4.7.5 Time Delay Logic

The time delay logic is shown at D-4 on sheet 3 and
serves two purposes:

* Generation of Power-on Reset
* Detection of Bus Time-out.

The logic consists of a 556 dual timer, with some
associated circuitry.

The Power-on Reset (POR) signal is generated
whenever the Reset Switch (RSTSW/) input from the
system bus is pulsed low or at power-on. The POR
signal is true for approximately 1 second.

The Bus Timeout (BUST/) signal is generated
whenever a period of 30-300 microseconds elapses
with the Address Strobe (AS/) signal occurring.
This usually indicates that the CPU is awaiting a
response from a peripheral which is either not
present or is unable to respond.

CHAPTER 5. MEMORY BOARDS

The Lisa provides a flexible memory configuration. The
physical memory space is divided into three spaces: main
memory, I/O space, and special I/O space.

The main memory occupies 2 Mbytes of space and is further
subdivided into two spaces of 1 Mbyte each, which correspond
to each of the two memory boards that may be present in the
Lisa. Each memory board is capable of sensing in which of the
two slots it is presently located because one pin of the board
socket is grounded on slot 2 and left open on slot 1. The
lower memory board occupies slot 2 and the higher occupies
slot 1.

In order to have memory that is contiguous, when each board
can not necessarily have a full 1 Mbyte available on it, a
scheme is implemented whereby both boards begin at their
mutual boundary of 100000@16 and fill outward from this point
to the capacity of the board.

To accommodate partially-stuffed boards and to maintain
interchangeability between slots, the physical top row of the
board in slot 2 (the lower board) must be the top of that
board's address space. Conversely, the top row of the board
in slot 1 (the upper board) must be the bottom of that board's
address space.

The amount of memory in slot 2 determines the physical
starting address of the memory available in the Lisa.
Likewise, the amount of memory in slot 1 defines the physical
ending address. Since the current memory boards are designed
around 64 Kbit dynamic RAMs, the smallest possible increments
are of 128 Kbytes each, or 64 Kwords of 16 bits each.

Because both the beginning and ending physical addresses are a
function of the amount of memory present, the boot ROM must
contain a routine that establishes the size and the location
of the memory available in each particular Lisa. The routine
must then configure the MMU RAM to place some part of the
physical address at logical address zero.

Since the memory boards can be installed in any order or
configuration, the operating system must add the required base
address when modifying the MMU RAM contents for any reason.

Note that the Video Page Address latch contains a physical
address, which must take the actual physical memory
configuration into account.

5.1   Memory Block Diagram

Since each memory board is functionally identical, this
section discusses the block diagram of a single board
only. A memory board consists of:

* An address decode section
* The memory matrix itself, and
* A parity detection and generation section.

The bulk of the memory control and timing signals are
generated on the processor board and provided on the
memory bus. Refer to section 4.6 for a discussion of
how these signals are generated. Figure 5-1 shows the
memory block diagram.

Figure 5-1. Memory Block Diagram

The matrix itself consists of four rows of eighteen 64 K
by 1 bit dynamic RAM devices. The extra 2 bits are used
as parity bits to check the integrity of data being read
from the memory.

Figure 5-1.   Memory Block Diagram

5-26
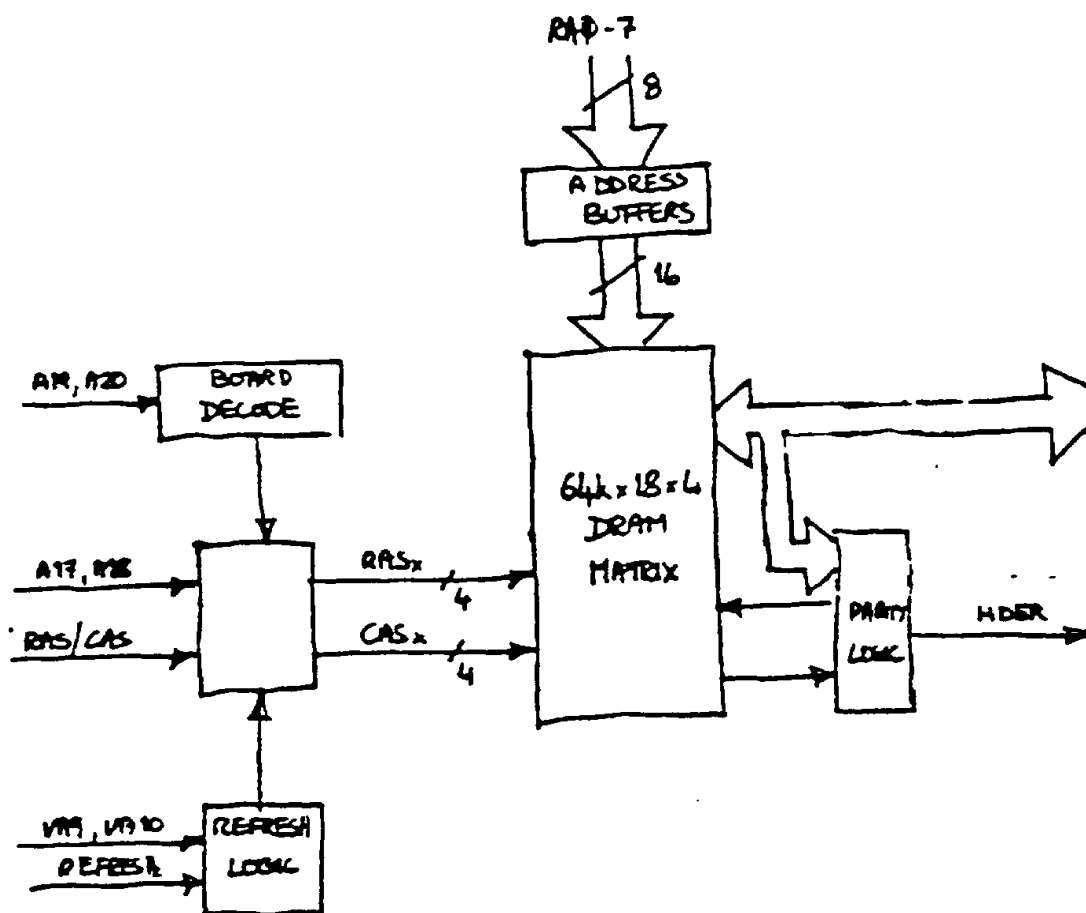
The parity logic both generates and checks the parity of
data being written and read respectively. The decode
logic is used to interpret the control signals to allow
the correct RAS and CAS signals to select the proper
row.

The latches and drivers are used to reduce loading on
certain critical signal lines.

5.2   Row and Column Addressing

The three types of memory accesses are CPU, video, and
DMA. The CPU and DMA accesses are identical, except for
some timing differences due to inconsistencies in the
DMA controller's reproduction of CPU signals. All
accesses appear identical to the memory board. The
address multiplexers on the processor board multiplex
not only the CPU/DMA address with the video address, but
also multiplex the matrix row address with the matrix
column address in sync with the row and column address
strobe signals.

5.2.1   Address Lines

The eight multiplexed address lines, RA1-RA8 at D-4
on sheet 1 of schematic Ø5Ø-4Ø1Ø in Appendix B, come
from the processor board via the memory bus on P1.
These are loaded into the dual S373 transparent
latches at D-3 in duplicate form by the LTCH/
signal.

The LTCH/ signal originates in the JK flop at C-3,
and is the DOTCK signal divided by two. It is
active only when CAS/ is deasserted to ensure that
the address for the RAMs is stable for a sufficient
period.

The address lines to the matrix consist of the
duplicated and latched RA1-RA8 signals, organized as
upper and lower address lines to minimize signal
loading and delay. These are shown at D-2 on sheet
1.

5.2.2   Slot Decode

The SLOT signal is shown at C-4 on sheet 1.
Depending on the slot in which the board is located,
this is pulled to GROUND in slot 2 (low-order board)
or allowed to be pulled up to +5 V in slot 1
(high-order board).

SLOT is presented to the matrix decode logic and
also to the pair of LS02 gates at C-3. The other
leg of these gates is a decode of the A19 and A20
terms by the LS139 decoder at B-3.

As can be seen from the connection of the Y1 and Y2
outputs to the gates, a logic high will be output
from the S32 gate at C-3 if either:

  * SLOT and& A20 are low while A19 is high
  * SLOT and& A20 are high while A19 is low.

This selects between the two boards using A19 and
A20. The addressing system is shown schematically
in Figure 5-2.

board	signal	row		
B1	CAS3	E	128 Kbytes	Upper 1M
B1	CAS2	D	128 Kbytes	fills
B1	CAS1	C	128 Kbytes	(SLOT 1)
B1	CAS0	B	128 Kbytes	upward
B2	CAS0	B	128 Kbytes	Lower 1M
B2	CAS1	C	128 Kbytes	fills
B2	CAS2	D	128 Kbytes	(SLOT 2)
B2	CAS3	E	128 Kbytes	downward

Figure 5-2. Memory Address Decoding

Note that the output signal from this section is
used to gate only the CAS signal to the matrix.
This is because no change is made to the contents of
RAM when a RAS-only cycle is performed.

5.2.3 Matrix Device Decode

The A17 and A18 signals from the memory bus are
presented to the S138 3-to-8 decoder at B-3. The
third input is the SLOT signal from the previous
subsection. This results in two groups of four
outputs, the high-order four for the high-order
board slot and the low-order four for the low-order
board slot.

These signals are presented to the two rows of gates
that follow, to allow memory to be physically
located next to the 1ØØØØØ@16 boundary discussed in
the introduction to this chapter.

Note that the RASØ/ output to the matrix on sheet 1
is a product of the Y4 decode output if SLOT is
high, but a product of the Y3 output if SLOT is
zero. That means that it corresponds to the
high-order block of the matrix in the low-order
slot, but the low-order block in the high-order
slot. Examination of all the other matrix strobe
signals will reveal a similar pattern.

5.2.4 Matrix Address Strobes

The RAS/ signal from the processor board enters the
memory board from the memory bus at A-4. It is used
to gate whichever of the inputs to the four SØØs at
A-2 has been enabled by the matrix decode logic,
described in the preceding subsection.

$$(SLOT/!.A2Ø/!.A19) \rightarrow SLOT\ 2$$

$$(SLOT!.A2Ø!.A19/) \rightarrow SLOT\ 1\ (high\ order)$$

$$(A17/!.A18/!.CAS/!.SLOT) + (A17!.A18!.CAS/!.SLOT/) \rightarrow CASØ/$$

$$(A17!.A18/!.CAS/!.SLOT) + (A17/!.A18!.CAS/!.SLOT/) \rightarrow CAS1/$$

$$(A17/!.A18!.CAS/!.SLOT) + (A17!.A18/!.CAS/!.SLOT/) \rightarrow CAS2/$$

$$(A17!.A18!.CAS/!.SLOT) + (A17/!.A18/!.CAS/!.SLOT/) \rightarrow CAS3/$$

This scheme permits the memory space to be filled
from the 1 Mbyte midpoint in both directions. This
eliminates gaps in the physical address space when
the full 2 Mbytes of memory are not installed.

The third input leg is to the SlØ gates at A-3 which
drives the SØØ's derives from the decode of VA9 and
VA1Ø from the LS139 2-to-4 decoder at A-3. This is
enabled by the Refresh (RFSH/) signal. Since the
video address register increments sequentially, it
is used to provide refresh.

The CAS/ signal from the processor board enters the
memory board at C-4 on sheet 1 and gates the

selected CASx signal, provided that the LS∅∅ gates
at B-3 are enabled.

Only one CASx/ will be active during any one
access. During a CPU or DMA access, only one RASx/
per board will be active, but in a video access, a
second RASx/ will be active to perform matrix
refresh.

5.3   Data and Parity

The logic concerned with data transfer and parity is
located on sheet 2 of schematic ∅5∅-4∅1∅. Parity is
stored in odd form for each byte in the memory matrix
and generates a hard memory error if read as an even
parity. Currently, there is no error correction
circuitry implemented in the Lisa memory. As a
consequence, soft memory errors are not corrected by the
memory board.

5.3.1 Memory Data Lines

The bidirectional data lines on the memory bus
MD∅-MD15 are connected directly to the DxIN inputs
of the matrix.

They are also connected to two LS28∅ parity
generator/checkers at C-3 and A-3, which generate
the odd parity for each of the upper and lower bytes
being written into memory. The EVEN outputs are
written into the corresponding bit in the matrix,
resulting in an 18-bit word being used to store the
two bytes, each with odd parity.

Data read from the matrix appear at the DxOUT
outputs, and are passed into the two LS373
transparent octal latches shown at A-2 and C-2. The
data are latched on the trailing edge of the main
RAS signal.

At the same time, the corresponding two parity bits
are latched into the LS375 shown at C-4 and A-4.
These are then gated with the MREAD signal to ensure
that the ninth bit is in fact stable during a write
operation before being presented to the parity
generator/checkers to establish if parity is good
for both bytes being read.

Output data are enabled onto the MD∅-MD15 lines of
the data bus by the S∅3 AND gate output at C-3.
This term is asserted if both MREAD and LBDSL are
asserted. The LBDSL originates at C-3 on sheet 1.

It shows that the board has been selected clocked on
the trailing edge of RAS.

A single byte can be written to or read from memory
under control of the LDS/ and UDS/ bus signals at
C-4 and A-4 respectively. The other half of the
memory word is read from memory, but is not passed
through the LS373.

5.3.2 Memory Parity

Odd, byte-wide parity is generated and tested in the
Lisa memory by means of two LS280 devices. Each
data byte has its own device associated with it.
The lower byte generates the PIL bit at C-2, while
the upper byte generates the PIU at A-2.

When a word is read from memory, the corresponding
two parity bytes are read and latched while the
parity is checked. For a word access, if either
byte results in an even parity, the JK flop at B-3
is set. This results in a HDER/ signal being
presented to the processor board to denote a memory
error. For a byte access, parity is checked only
for the byte being accessed. The parity of the
other byte is ignored.

The HDER/ signal is also fed back into the parity
logic for use in parity diagnostics. Note that it
is also latched until a write operation is performed
to clear this.

If a parity error occurs during video access to
memory, it is reported to the CPU 60 times per
second until the parity is remasked or the word
causing the error is rewritten. This is true even
if the CPU itself never accesses the memory location
causing the parity error.

5.3.3 Memory Refresh

Refresh cycles occur during a video access by
selecting multiple rows of memory devices on the
board. Since the video addresses cycle through all
device-row addresses every 128 accesses, this
feature is used in place of a separate hardware
refresh address generator.

The upper and lower halves of 64 Kbit RAM devices
are selected by the polarity of the RA8 input at RAS
time. RAM devices that require refresh every 128
cycles have their upper and lower halves refreshed

simultaneously and therefore require only 2
milliseconds for full refresh. RAM devices that
require refresh every 256 cycles need the full 4
milliseconds refresh cycle time for full refresh.

Refresh alternates between installed memory boards
every 128 cycles. The order of alternation is
reversed after every refresh pass in order to supply
the correct refresh to 256-cycle refresh RAMs,
should these be installed. This is done by means of
the VA8 and VA11 signals from the processor board
and results in the pattern shown in Figure 5-3.

```
------------------------------------------------
        Board Ø, Row Ø, Lower half         ^
                                           |
        Board 1, Row Ø, Upper half         |
                                           |
        Board Ø, Row 1, Lower half         |
                                           |
        Board 1, Row 1, Upper half         |
                                        2 milliseconds
        Board Ø, Row 2, Lower half         |
                                           |
        Board 1, Row 2, Upper half         |
                                           |
        Board Ø, Row 3, Lower half         |
                                           |
        Board 1, Row 3, Upper half         v
_____   <- Order reverses
        Board 1, Row Ø, Lower half         ^
                                           |
        Board Ø, Row Ø, Upper half         |
                                           |
        Board 1, Row 1, Lower half         |
                                           |
        Board Ø, Row 1, Upper half         |
                                        2 milliseconds
        Board 1, Row 2, Lower half         |
                                           |
        Board Ø, Row 2, Upper half         |
                                           |
        Board 1, Row 3, Lower half         |
                                           |
        Board Ø, Row 3, Upper half         v
_____
```

Pattern repeats from the top

Figure 5-3. Memory Refresh Pattern

5.4   Memory Timing

As with most systems, the timing associated with memory
access is one of the critical constraints around which
the computer has been designed. The timing diagram for
the memory board is shown in Figure 5-4.

Figure 5-4. Memory Timing Diagram

5.4.1 Row Selection Timing

The most critical timing in the memory involves the
decode of the A17 and A18 address lines. Both these
lines are the product of the address translation
within the MMU on the processor board, and
consequently reach the memory board with some delay
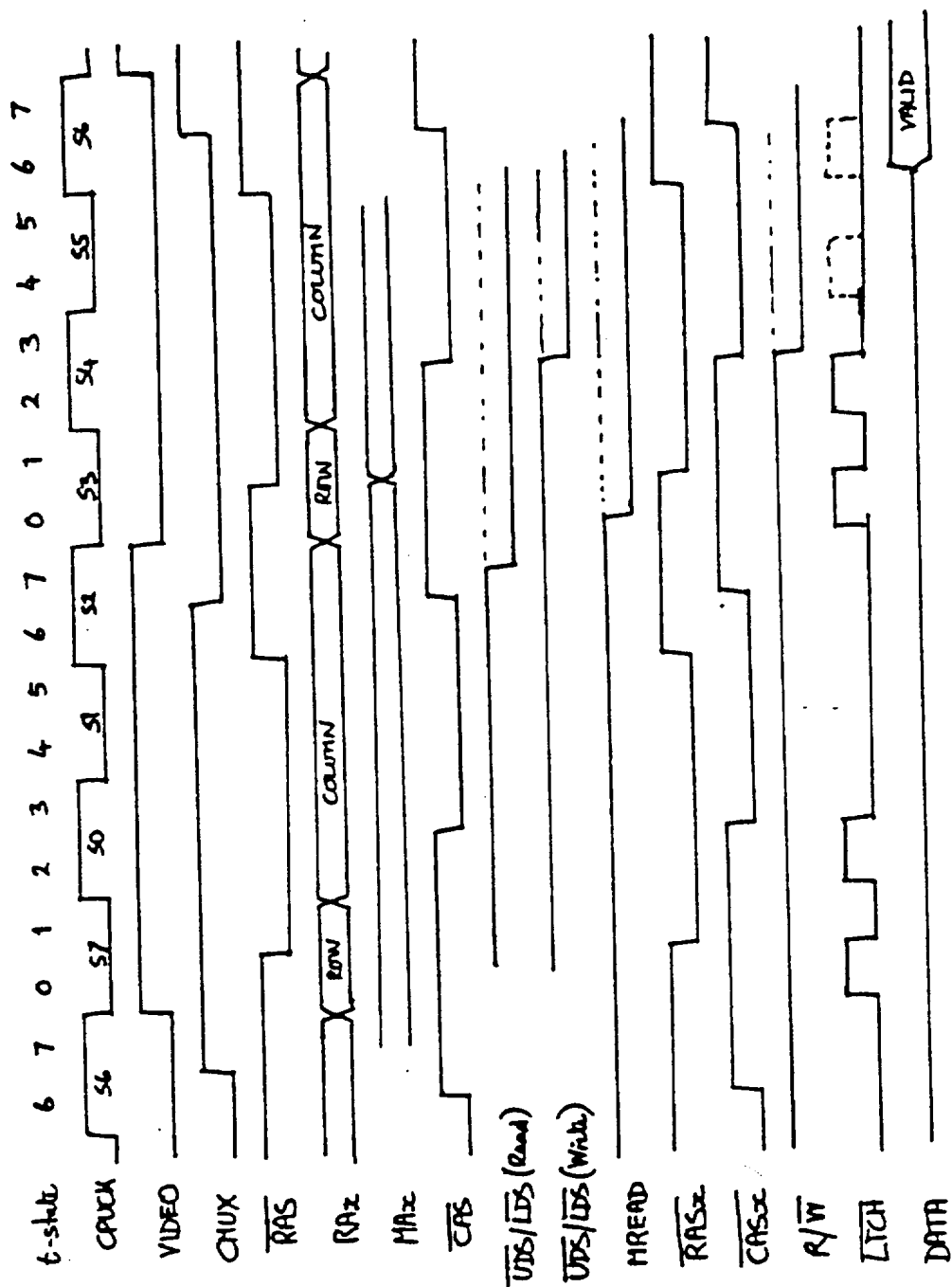
Figure 5-4. LISA Memory Timing Diagram

9b
5-10e

after the AS/ signal that begins the cycle. Since
these signals are also used to generate the correct
RASx/ signal within the matrix, it might not be
possible to select the board before RAS time.

The difficulty is solved by generating RAS on both
boards in any case and using the CAS signal to
define which part of the matrix is in fact being
accessed. This is shown in Figure 5-5.

Figure 5-5. Memory Row Address Timing

5.4.2 Address Multiplex Timing

In order for the correct word in memory to be
accessed, the address is presented to the matrix in
two halves. This is also shown in Figure 5-5.

The two halves correspond to the row address and the
column address of the word being accessed. The
processor board makes each of these available in
turn on the RA1-RA8 lines. It uses the RAS/ or CAS/
signals to strobe the address.

The multiplexed address is latched into the S373s
with the LTCH/ term. This has the waveform shown in
Figures 5-4 and 5-6. The flop generating it toggles
at the frequency of DOTCK whenever the CAS/ term is
deasserted. Otherwise, it remains asserted.
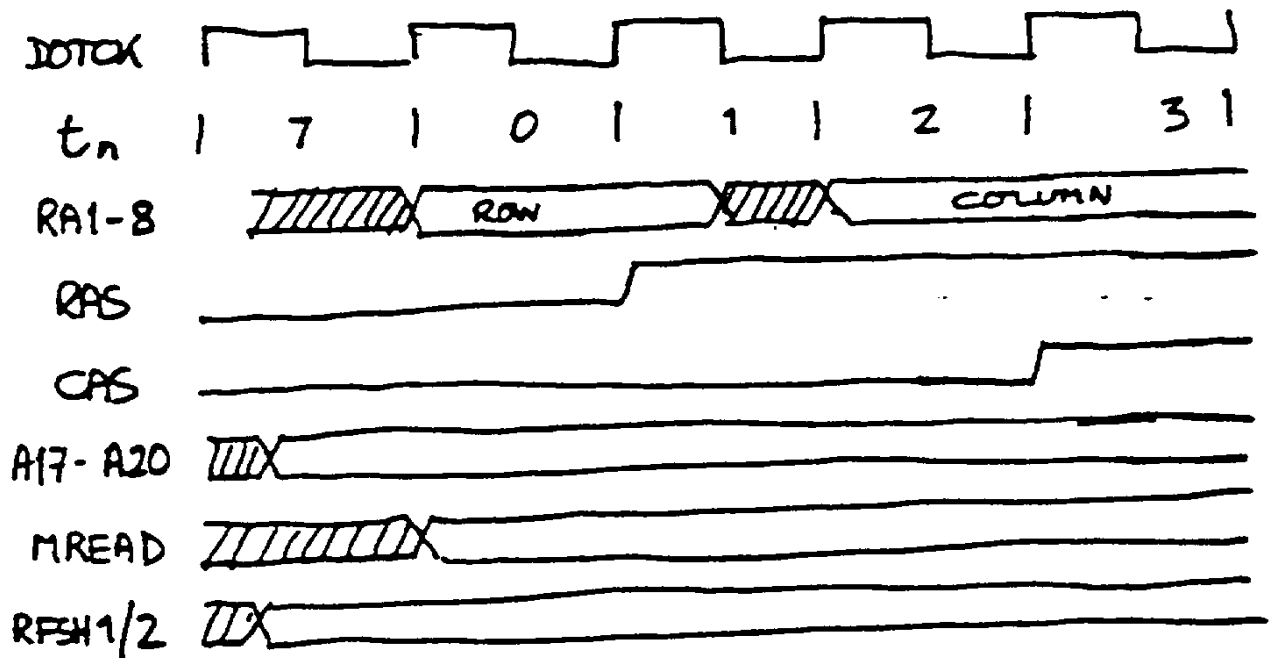
Figure 5-5. Memory Row Address Timing

5-10b

Lisa Hardware Manual

5.4.3 Data and Parity Timing

The constraints on the data and parity signals of the matrix are less rigorous than those for the address selection. The timing is shown in Figure 5-6.

Figure 5-6. Memory Data and Parity Timing

Figure 5-6. Memory Data and Parity Timing

5-13c
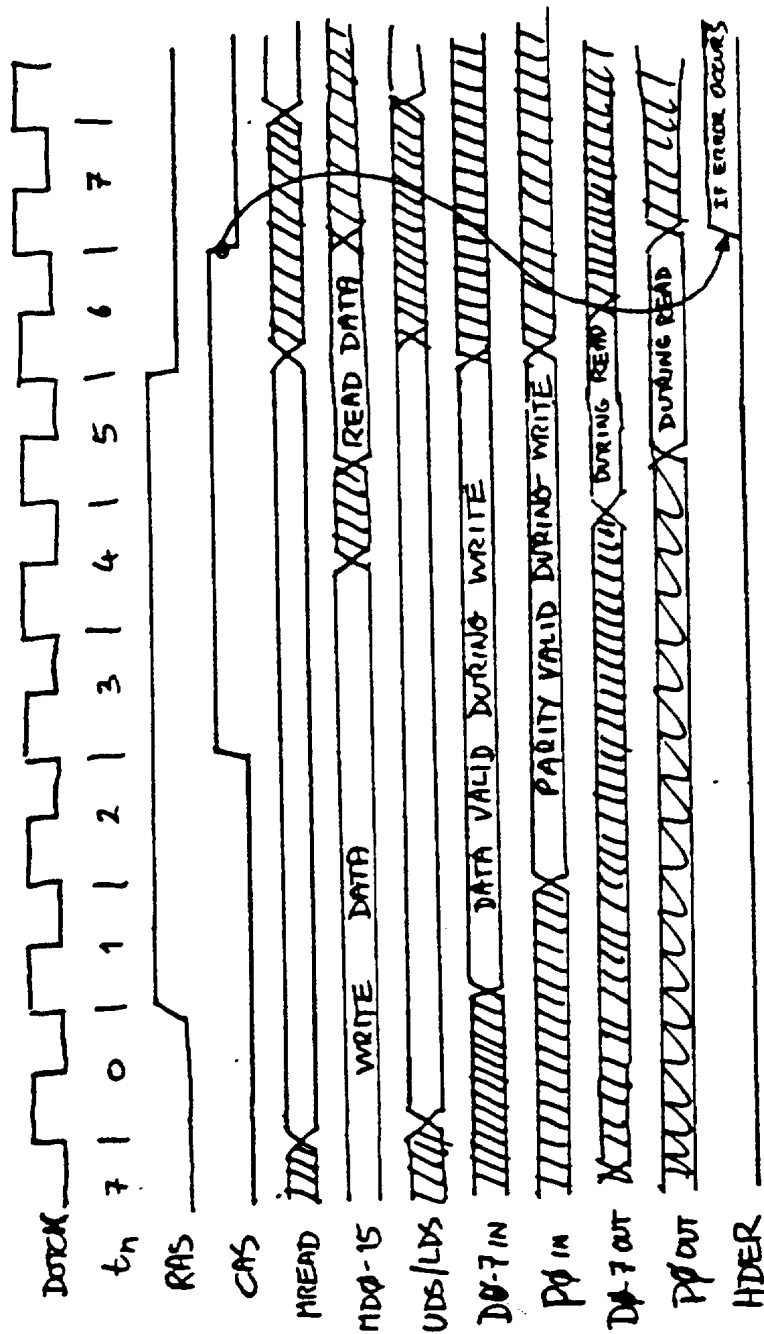
CHAPTER 6. THE I/O BOARD

The Lisa communicates with its peripherals principally through
the I/O board, which contains the peripheral controllers for
the external interface connectors of the Lisa. The I/O board
must be present in any Lisa.

6.1   I/O Board Block Diagram

The main features on the I/O board are shown in Figure
6-1 and can be itemized as follows:

  * Floppy-disk controller
  * Two serial I/O port interfaces
  * A parallel port interface
  * Keyboard/Mouse interface
  * Miscellaneous logic.

The data bus on the I/O board consists of three separate
sections, which are also shown in Figure 6-1. These are
the:

  * System-bus data lines from off-board,

  * Disk bus, internal to the floppy-disk
    controller,

  * D-bus connecting to all other peripherals.

Note that some control functions are grouped together on
the same interface device. This is done both for
convenience and to minimize hardware.

Figure 6-1. I/O Board Block Diagram

6.2   Floppy-Disk Controller

       The floppy-disk controller is designed around a 65Ø4A
       processor and its associated memory and logic. Figure
       6-2 shows a block diagram of the floppy-disk
       controller. Operation of the controller is described in
       section 6.3; The logic schematic can be found on sheet 4
       of schematic Ø5Ø-4ØØ8 in Appendix C.
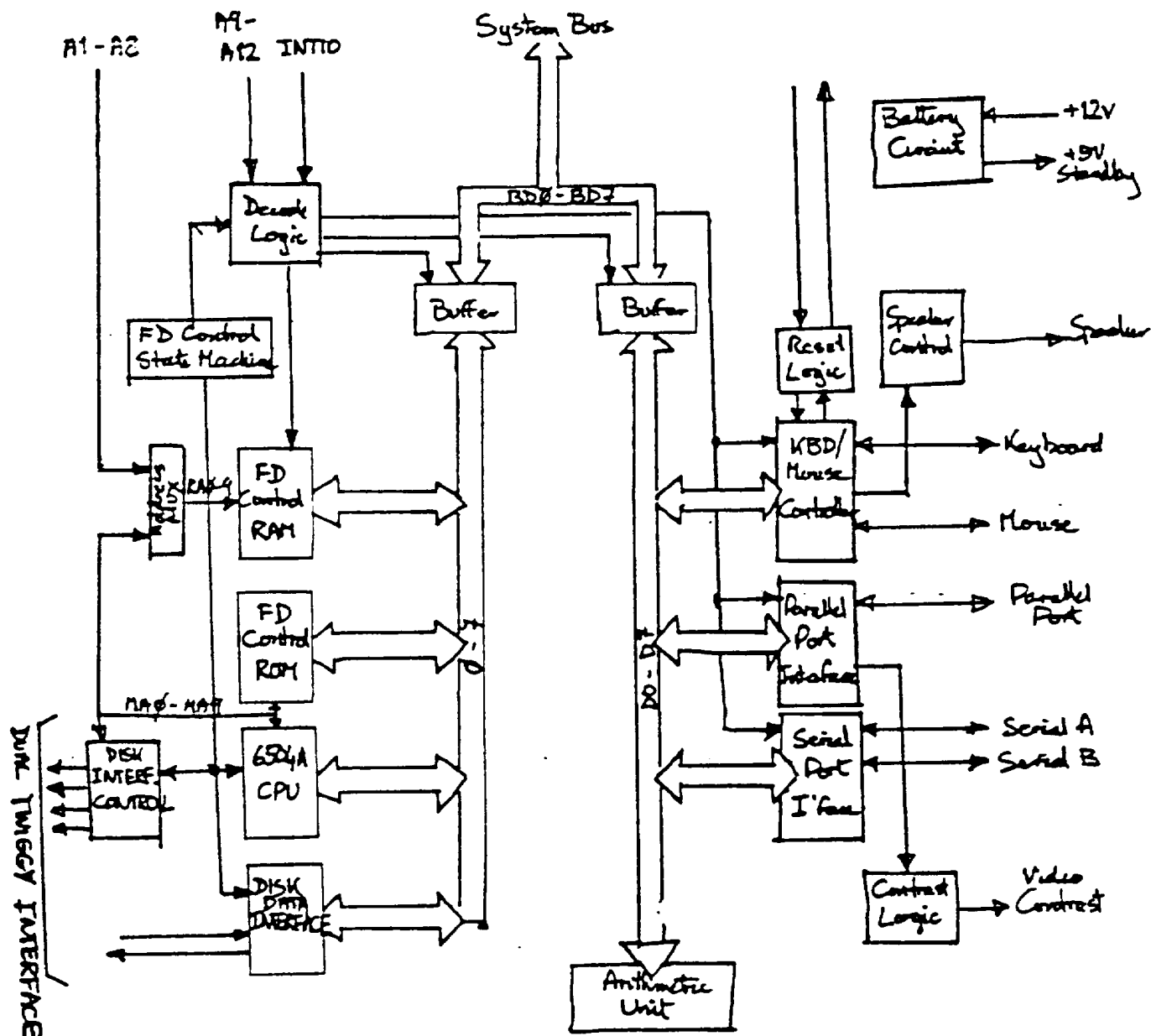
Figure 6-1.   I/O Board Block Diagram

6-2b

Figure 6-2. Floppy-Disk Controller Block Diagram

The controller communicates with the Lisa through an
area in its dedicated memory. The CPU places commands
and data to be written on the disk at locations in this
RAM. The CPU can also access status information and
data read from the disk that is placed in the RAM by the
processor.

Timing for the controller is generated asynchronously to
the 68000 by a clock generator internal to the
controller. This provides clocking to the processor and
to control latches.

The control lines to the two floppy-disk drives are
generated by addressable latches that are loaded by
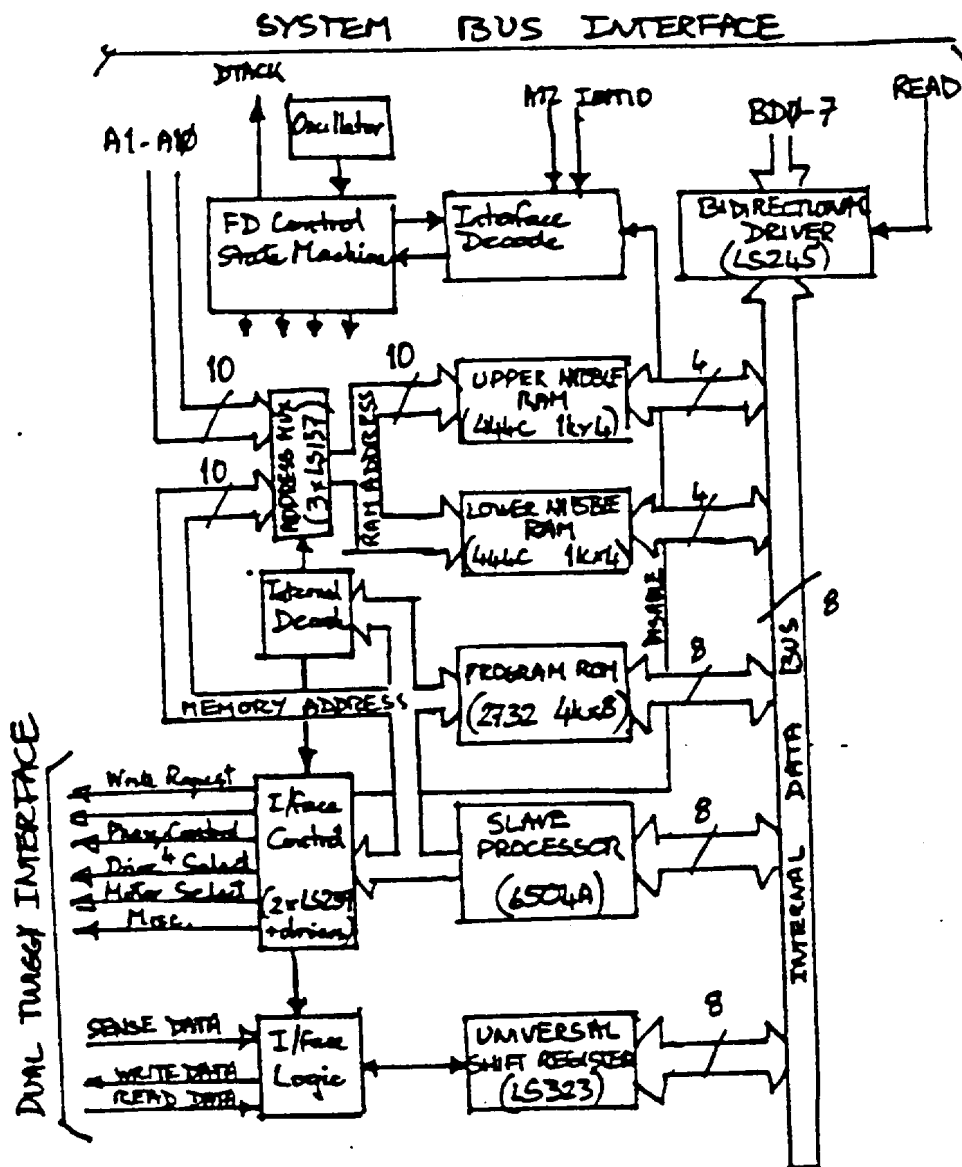
Figure 6-2. Floppy Disk Controller Block Diagram

$$\frac{3b}{6-4e}$$

slave processor operation. The data interface to the
drives is controlled by a state machine, which is used
to monitor and control this interface under control of
the 65Ø4A.

6.2.1 Processor and Memory

The heart of the controller is a 65Ø4A 8-bit
processor at D-3, which accesses two types of
memory. A 4 K by 8 program ROM at D-3 contains the
processor control routines with which it performs
manipulation of the interface to the two floppy-disk
drives and also transfer of data to and from the
main processor.

Data being transferred is stored in the two parallel
1 K by 4 RAM devices at D-3 and D-4. These provide
a 1 Kbyte buffer space, common to both the 65Ø4A and
the main processor, for use as a data buffer. The
RAM is also used for storing command strings from
the processor to the controller and for status
information from the disk. The RAM is functionally
divided as shown in Figure 6-3.

Figure 6-3. Floppy-Disk Controller Address Space

The bidirectional LS245 octal buffer at D-4 divides the
internal floppy-disk controller data bus from the system
bus data lines BD∅-BD7. The internal bus connects to
the 2732 PROM, the 65∅4A processor, and the upper and
lower nibbles are connected to one 444C RAM each. In
addition, the bus connects to the LS323 universal shift
register at D-2.

The 8 Kbyte address space of the processor is addressed
by means of the internal address bus MA∅-MA12. These
connect directly to the program ROM and are multiplexed
with system bus address lines for accesses to the buffer
RAM.

```
0000 ┌──────────────────────────────────┐
     │  IOB (Input/Output Control Block)│
     │     (see  Figure  6-8 )          │
0010 ├──────────────────────────────────┤
     │  R/W Shared RAM  (Initialized    │
     │                   by the 6504)   │
0020 ├──────────────────────────────────┤
     │  6504 Status Block  (Read-only   │
     │                      for the 68000)│
0030 ├──────────────────────────────────┤
     │  Internal IOB      (Used only    │
     │                     by the 6504  │
0040 ├──────────────────────────────────┤
     │                                  │
     │  6504 Internal Variables         │
     │           (Global and Local )    │
     │                                  │
     │                                  │
     │                                  │
00C0 ├──────────────────────────────────┤
     │                                  │
     │  LISA Parameter Storage          │
     │                                  │
     │              (Used only          │
     │               by the 68000 )     │
0100 ├──────────────────────────────────┤
     │  6504 Stack                      │
     │                         ↑        │
     │              (Used in   │        │
     │               this order)        │
0180 ├──────────────────────────────────┤
     │  6504 General Storage Area       │
     │                                  │
     │                                  │
01F4 ├──────────────────────────────────┤
     │  I/O Buffer                      │
     │                                  │
     │            (524 bytes)           │
05FF └──────────────────────────────────┘
```

Figure 6-3. Floppy Disk Controller Address Space

6-5b

The internal memory bus is also used to select the
control lines to be manipulated on the disk interface
via the LS259 selectable latches at B-1 and C-2. It
provides internal decodes using the LS139 dual 2-to-4
decoder shown at B-2 and B-3.

6.2.2 System Bus Interface

The interface to the system bus consists of the
devices shown on the left side of sheet 4 of the
schematic, that is, the bidirectional data bus
transceiver at D-4, the three LS157 2-to-1
Multiplexer devices at C-4 to A-4, and some control
circuitry at A-3 and A-4.

The processor is capable of locking out any
communication on the main bus by means of the DIS
signal. This is done because many routines within
the disk controller are time-critical. Accesses
from the 68000 would render them impossible.

DIS is one of the inputs to the LS32 gates at A-3.
When this signal is asserted, the J input of the JK
flop at A-3 is always asserted. This means that the
output is always true, and that the second JK flop
at A-3 is always set, giving an output at pin 6
which is always asserted. This forces the S input
on the LS157 Multiplexer to select the MAx inputs at
all times and disables the bus transceiver at D-4.

The Q/ output of the second LS109 flop at A-3 is
gated into another LS109 JK flop at A-2. This
generates the DTACK/ signal on the system bus only
if the Q/ output from A-3 is high. This can happen
only when DIS is deasserted.

Thus any attempt to communicate with the controller
while DIS is high does not result in a DTACK/
acknowledgement signal. The access cycle hangs,
waiting for this signal until the bus timeout on the
processor board triggers and the BERR/ signal is
generated. Refer to section 4.7 for a discussion of
this.

Note that the DTACK/ signal is generated by an LS367
tristate driver device, which is enabled only when
the Flop at A-3 Q output is low.

6.2.3 Timing Generation

The floppy-disk controller runs asynchronously to
the Lisa. Its timing is controlled by logic built

around an LS161A 4-bit counter.

Timing is provided by a 16 MHz oscillator, located
at B-3 on sheet 4 of schematic 050-4008. The output
is buffered by the Schmitt trigger NAND gates before
being presented to the LS161A counter at B-3. Pin 5
of device U6A may be used to provide an alternative
clock input if pin 1 is pulled to ground to disable
the normal clock.

The timing state sequence that the counter passes
through is dependent on whether the controller is
communicating with the processor or performing
internal control functions with the processor locked
out. The state machine goes through eight states in
the former case and nine in the latter. Refer to
Figure 6-4 for an overview of the states that are
passed through.

Figure 6-4. Floppy-Disk Counter Timing States

If the controller is communicating with the
processor, the DIS signal is deasserted. This means
that the LS109 JK flop at A-3 is in the reset
condition, resulting in a low condition on the P0
input to the LS161A at B-2.

$Q_D\ Q_C\ Q_B\ Q_A$

```
  ┌─ system →1 0 0 0      Start for system control loop
  ├─ local →1 0 0 1       Start for local control loop.
  │        1 0 1 0        Wait state (waits for AS/ asserted)
  │        1 0 1 1
  │        1 1 0 0
  │        1 1 0 1
  │        1 1 1 0
  │        1 1 1 1
  └─────── 0 0 0 0        Perform Start Load.
```

↑

└ phi ∅ clock to 6504 Slave Processor
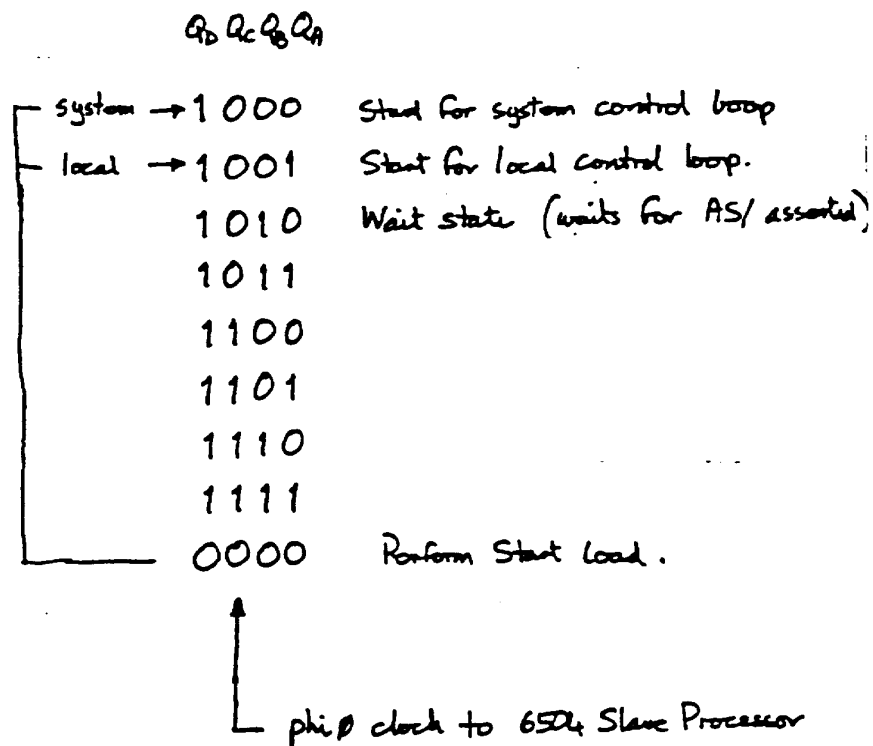
Figure 6-4.   FD Counter Timing States

6-78

When the counter rolls over to zero, the Q3 output
goes low and causes the P-inputs to be loaded. In
this case, an 8 is loaded, since the P3 input is
pulled high and all other inputs are low. At this
point, the Q1 output is low, which results in the
CEP input being asserted. Since the CET input is
pulled high, the counter is enabled and begins to
count.

The clock input is running and the machine will
clock up from state 8 to 9. This causes the Q0
output to go high and to sample whether the CPU is
attempting to access the controller by clocking the
lower LS109 JK flop at A-3. The Q output becomes
deasserted in this case, which enables the DTACK
driver at A-2. It is also presented to the upper
flop at A-3, which acts as the internal mode
selector and uses the 6504A's phi2 clock to present
a high to pin 4 of the LS00 at A-2.

When the counter clocks from 9 to 10, the Q1 output
goes high, which presents a low input to the j input
of the LS109 JK flop at A-2. This in turn asserts
the DTACK/ signal to the processor to initiate the
I/O data transfer cycle. This also deasserts the
CEP input to the counter, which means that the
counter and thus the entire controller hangs waiting
for the processor to respond.

Processor response is detected by the AS signal.
When this is deasserted, the upper flop at A-3 is
preset, which drives the CEP to its asserted state
again. The AS also presets the lower flop, which
disables the DTACK/ signal. The counter then
proceeds in sequence through states 11 to 15 before
rolling over and beginning the sequence again.

In the case where the processor is not attempting to
access the controller, the lower flop at A-3 is
set. This causes the counter to begin in state 9,
since the P0 input is high when the PE load signal
is asserted.

The Q0 output is solely used to clock the disable
flop at A-3. Due to the asynchronous nature of this
clocking with the interface, the second flop at B-3
has been added to give a stable period to the
state.

The Q1 output performs two functions. First, it is
used as a clock to drive the disk state machine at
D-1 and D-2. Second, it is used as a gating term
for the DTACK flop at A-2, which also halts the
counter to wait for processor response.

The Q2 output is only used to provide the input
clock to the processor at C-2. This defines the
period of the phi2 clock output by the processor.

The Q3 output is used exclusively to reset the
counter to its initial count state.

The phi2 clock from the 6502A is used to clock the
upper flop at A-2 and also to provide timing for
loading the control latches at B-1 and C-2.

6.2.4 Disk State Machine

The interface to the drive itself includes a state
machine whose purpose it is to perform the data
parallel/serial translation during transfer to and
from the drive.

The state machine consists of three devices, as
shown in Figure 6-5. The central device is a 256-
by 8-bit ROM at D-2, which works in conjunction with
the hex D-Flop LS174 at D-1 and the 74LS323 8-bit
universal shift register at D-2.

September 7th 1982

CLR	S1	S0	Operation	Used to perform
1	0	0	Hold	Present data to controller
1	0	1	Shift Left	Receive data from disk
1	1	0	Shift right	Present data to disk
1	1	1	Load.	Receive data from controller
0	x	x	Clear.	

Q_A holds MSB. When it is a "1", the byte is assembled.
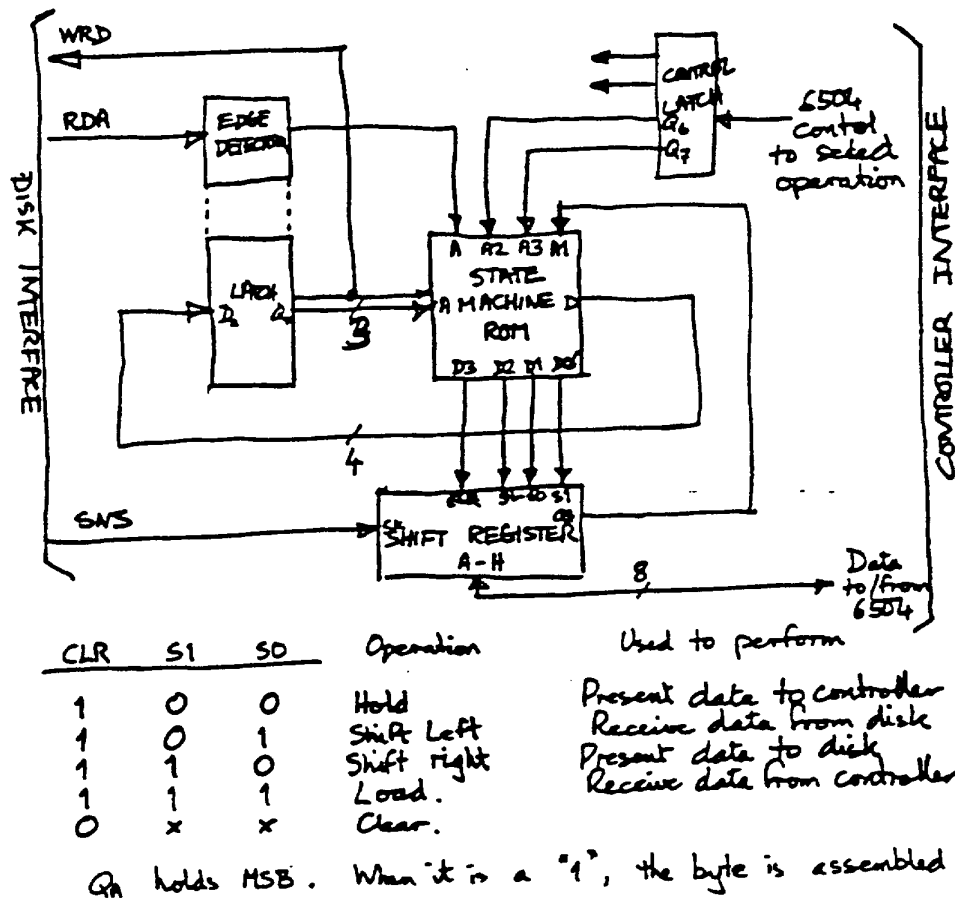
Figure 6-5.   Disk State Machine

9b
6-11e

~~Figure 6-5. Disk State Machine~~

The processor uses two outputs of the LS259 to
select one of four operations within the state
machine. In addition, data are made available on
the internal controller data bus for parallel
loading into the shift register.

The state machine is clocked by the Q2 output of the
timing counter described in subsection 6.2.3 above.

The interface signals that connect to this section
of the logic are as follows:

> RDA is input from the drive and is the Read
> Data line containing serial data from the
> selected head and drive.

> WRD is output to the drive and is the Write
> Data line for the serial data written by the
> selected drive and head.

> SNS is input from the drive and is the sense
> line that presents the selected status
> information on the floppy-disk drive system.

6.2.5 Stepper Motor Control

The control of the stepper motor in the drives is
performed with the LS259 8-bit addressable latch at
C-2. The various bits are selected by means of the
low-order internal controller address lines.

These are passed through line drivers to provide the
following signals. Note that the first two signals
do not actually control stepper movement. The
signals are:

> WRQ/ is the Write Request line, which is
> output to the drive to permit write
> operations to be performed.

> HDS is the Head Select line, which is output
> to the drive to indicate which of the two
> heads on the selected drive is to be used to
> write or read data. It also is used to
> select which status data are to be read on
> the sense line.

> phi0-phi3 are the four phase control lines
> output to the drive to control the carriage

motion performed by the stepper motor. In
addition, the phi∅ signal is used in the
selection of status data read on the sense
line.

The first two signals are placed here only for
convenience. The motor phase control line operation
is described in subsection 6.3.5

6.2.6 General Drive Control

The function of the general drive control logic is
to manipulate lines on the drive interface. This is
performed by the LS259 8-bit addressable latch at
B-1 with some additional logic.

The latched bits are addressed by the low-order four
lines on the internal controller address bus.

Two bits are used to provide information to the
CPU:

FDIR is the Floppy-Disk Interrupt Request.
It is fed into the inverting driver shown at
B-4 on sheet 3 where it generates the IOIR/
interrupt request to the processor. It is
also presented to the PB4 inputs of the
keyboard interface device for polling by the
CPU.

DSKDIAG is the Disk Diagnostic line that is
presented to the PB7 input of the parallel
port interface device for polling by the CPU
to indicate that the controller is performing
disk diagnostics.

One bit is used for internal control on the I/O
board:

Disable (DIS) is the control signal that the
65∅4A uses to inhibit the interface to the
68∅∅∅ when it is the process of an operation
which must not be interrupted.

Four bits are used as control signals to the disk
drives:

MT∅/ & MT1/ are the motor control lines,
which output to the two individual disk
drives to control the spindle rotation

speed.

DR∅/ & DR1/ are the drive select lines, which
select between the two drives in the dual
drive assembly.

6.3   Floppy-Disk Controller Operation

The floppy-disk controller manipulates the control
lines to the drives to read data from and write data
to all tracks and surfaces of the disk drive. It
communicates with the CPU by means of a common RAM
space on the I/O board, shown in Figure 6-3.

The CPU requests the floppy-disk controller to
perform operations by means of commands placed in
the GOBYTE in location ∅∅∅∅@2, plus other parameters
within the I/O block as required. The 65∅4 command
structure is shown in Figures 6-6a through 6-6r.

■ Issued   ▤ Returned   (HANDSHAKE)

6504	68000	DESCRIPTOR	RANGE	COMMENT
0000	FCC001	gobyte	80	handshake, zeroed
0001	FCC003	function	00	
0002	FCC005	drive	00, 80	00 = top
0003	FCC007	side	00, 01	00 = top
0004	FCC009	sector	00..15	see below*
0005	FCC00B	track	00..2D	00 = outer
0006	FCC00D	speed	DA..23	00 = norm, DA = fast
0007	FCC00F	confirm	FF	
0008	FCC011	status	00..1C	00 = no error
0009	FCC013	dsk ID	00..02	00 duo, 01 lisa, 02 mac
002C	FCC059	retry -	00..64	64 = no retrys
005B	FCC0B7	dat bitslp1	00..FF	00 = no error
005C	FCC0B9	dat bitslp2	00..FF	00 = no error
005D	FCC0BB	dat chksm	00..FF	00 = no error
005E	FCC0BD	adr bitslp1	00..01	00 = no error
005F	FCC0BF	adr bitslp2	00..FF	00 = no error
0060	FCC0C1	wrong sec	00..FF	00 = no error
0061	FCC0C3	wrong trk	00..01	00 = no error
0062	FCC0C5	adr chksm	00..FF	00 = no error
007E	FCC0FD	usr chksm	00..FF	user
007F	FCC0FF	usr chksm	00..FF	user
0080	FCC101	usr chksm	00..FF	user
01D0	FCC3A1	bad sec total	00..max sector	error only
01D1	FCC3A3	error trk #	00..max track	error only
01D2	FCC3A5	error side #	00, 01	error only
01D3	FCC3A7	bad sector map	00..max sector	error only
01F4	FCC3E9	buf begin		R/W data
03FF	FCC7FF	buf end		
COPS PB=4	FCDD81	FDIR	digital bit	high = interrupt pending
Parallel PB=6	FCC901	DSKDIAG	digital bit	low = busy

FCD

Pre issue requirements: DSKDIAG high
                                 gobyte zeroed

Post issue memory access: no special requirements
                            gobyte zeroed on handshake

**
tracks/sectors	tracks/sectors
0-3 / 0-15	17-1C / 0-11
4-A / 0-14	1D-22 / 0-10
B-10 / 0-13	23-29 / 0-F
11-16 / 0-12	2A-2D / 0-E

**ALL VALUES ON THIS PAGE ARE HEX

Figure 6-6a. (FD) Controller Handshake Command

Floppy - Disk [config.]

6-13

■ Issued   🖵 Returned   (READ)

6504	68000	DESCRIPTOR	RANGE	COMMENT
0000	FCC001	gobyte	81	RWTS, zeroed
0001	FCC003	function	00	read
0002	FCC005	drive	00, 80	00 = top
0003	FCC007	side	00, 01	00 = top
0004	FCC009	sector	00..15	see below**
0005	FCC00B	track	00..2D	00 = outer
0006	FCC00D	speed	DA..23	00 = norm, DA = fast
0007	FCC00F	confirm	FF	format confirmation
0008	FCC011	status	00..1C	00 = no error
0009	FCC013	dsk ID	00..02	00 duo, 01 lisa, 02 mac
002C	FCC059	retry	00..64	64 = no retrys
005B	FCC0B7	dat bitslp1	00..FF	00 = no error
005C	FCC0B9	dat bitslp2	00..FF	00 = no error
005D	FCC0BB	dat chksm	00..FF	00 = no error
005E	FCC0BD	adr bitslp1	00..FF/01	00 = no error
005F	FCC0BF	adr bitslp2	00..FF	00 = no error
0060	FCC0C1	wrong sec	00..FF	00 = no error
0061	FCC0C3	wrong trk	00..FF/01	00 = no error
0062	FCC0C5	adr chksm	00..FF	00 = no error
007E	FCC0FD	usr chksm	00..FF	user
007F	FCC0FF	usr chksm	00..FF	user
0080	FCC101	usr chksm	00..FF	user
01D0	FCC3A1	bad sec total	00..max sector	error only
01D1	FCC3A3	error trk #	00..max track	error only
01D2	FCC3A5	error side #	00, 01	error only
01D3	FCC3A7	bad sector map	00..max sector	error only
01F4	FCC3E9	buf begin		R/W data
03FF	FCC7FF	buf end		
COPS PB=4	FCDD81	FDIR	digital bit	high = interrupt pending
Parallel PB=6	FCC901	DSKDIAG	digital bit	low = busy

FCD

Pre issue requirements: DSKDIAG high
                               drive enabled
                               gobyte zeroed
                               no interrupts pending

Post issue memory access: none until FDIR

* tracks/sectors	tracks/sectors
0-3 / 0-15	17-1C / 0-11
4-A / 0-14	1D-22 / 0-10
B-10 / 0-13	23-29 / 0-F
11-16 / 0-12	2A-2D / 0-E

**ALL VALUES ON THIS PAGE ARE HEX

Figure 6-6b. FD Controller Read Command

September 7th 1982   LISA Hardware Manual

■ Issued   ▣ Returned   WRITE

6504	68000	DESCRIPTOR	RANGE	COMMENT
0000	FCC001	gobyte	81	RWTS, zeroed
0001	FCC003	function	01	write
0002	FCC005	drive	00, 80	00 = top
0003	FCC007	side	00, 01	00 = top
0004	FCC009	sector	00..15	see below*
0005	FCC00B	track	00..2D	00 = outer
0006	FCC00D	speed	DA..23	00 = norm, DA = fast
0007	FCC00F	confirm	FF	format confirmation
0008	FCC011	status	00..1C	00 = no error
0009	FCC013	dsk ID	00..02	00 duo, 01 lisa, 02 mac
002C	FCC059	retry	00..64	64 = no retrys
005B	FCC0B7	dat bitslp1	00..FF	00 = no error
005C	FCC0B9	dat bitslp2	00..FF	00 = no error
005D	FCC0BB	dat chksm	00..FF	00 = no error
005E	FCC0BD	adr bitslp1	00..00 01	00 = no error
005F	FCC0BF	adr bitslp2	00..FF	00 = no error
0060	FCC0C1	wrong sec	00..FF	00 = no error
0061	FCC0C3	wrong trk	00..00 01	00 = no error
0062	FCC0C5	adr chksm	00..FF	00 = no error
007E	FCC0FD	usr chksm	00..FF	user
007F	FCC0FF	usr chksm	00..FF	user
0080	FCC101	usr chksm	00..FF	user
01D0	FCC3A1	bad sec total	00..max sector	error only
01D1	FCC3A3	error trk #	00..max track	error only
01D2	FCC3A5	error side #	00, 01	error only
01D3	FCC3A7	bad sector map	00..max sector	error only
01F4	FCC3E9	buf begin		R/W data
03FF	FCC7FF	buf end		
COPS PB=4	FCDD81	FDIR	digital bit	high = interrupt pending
Parallel PB=6	FC6901	DSKDIAG	digital bit	low = busy

FCD

Pre issue requirements: DSKDIAG high
                               drive enabled
                               gobyte zeroed
                               no interrupts pending

Post issue memory access: none until FDIR

**	tracks/sectors	tracks/sectors
	0-3 / 0-15	17-1C / 0-11
	4-A / 0-14	1D-22 / 0-10
	B-10 / 0-13	23-29 / 0-F
	11-16 / 0-12	2A-2D / 0-E

**ALL VALUES ON THIS PAGE ARE HEX

Figure 6-6c. FD Controller Write Command

6-18

▣ Issued   ▤ Returned   [UNCLAMP]

6504	68000	DESCRIPTOR	RANGE	COMMENT
0000	FCC001	gobyte	81	RWTS, zeroed
0001	FCC003	function	02	unclamp
0002	FCC005	drive	00, 80	00 = top
0003	FCC007	side	00, 01	00 = top
0004	FCC009	sector	00..15	see below**
0005	FCC00B	track	00..2D	00 = outer
0006	FCC00D	speed	DA..23	00 = norm, DA = fast
0007	FCC00F	confirm	FF	format confirmation
0008	FCC011	status	00..1C	00 = no error
0009	FCC013	dsk ID	00..02	00 duo, 01 lisa, 02 mac
002C	FCC059	retry	00..64	64 = no retrys
005B	FCC0B7	dat bitslp1	00..FF	00 = no error
005C	FCC0B9	dat bitslp2	00..FF	00 = no error
005D	FCC0BB	dat chksm	00..FF	00 = no error
005E	FCC0BD	adr bitslp1	00..FF 01	00 = no error
005F	FCC0BF	adr bitslp2	00..FF	00 = no error
0060	FCC0C1	wrong sec	00..FF	00 = no error
0061	FCC0C3	wrong trk	00..FF 01	00 = no error
0062	FCC0C5	adr chksm	00..FF	00 = no error
007E	FCC0FD	usr chksm	00..FF	user
007F	FCC0FF	usr chksm	00..FF	user
0080	FCC101	usr chksm	00..FF	user
01D0	FCC3A1	bad sec total	00..max sector	error only
01D1	FCC3A3	error trk #	00..max track	error only
01D2	FCC3A5	error side #	00, 01	error only
01D3	FCC3A7	bad sector map	00..max sector	error only
01F4	FCC3E9	buf begin		R/W data
03FF	FCC7FF	buf end		
COPS PB=4	FCDD81	FDIR	digital bit	high = interrupt pending
Parallel PB=6	FCE901	DSKDIAG	digital bit	low = busy

FCD

Pre issue requirements:	DSKDIAG high
	drive enabled
	gobyte zeroed
	no interrupts pending
Post issue memory access:	none until FDIR

※	tracks/sectors	tracks/sectors
	0-3 / 0-15	17-1C / 0-11
	4-A / 0-14	1D-22 / 0-10
	B-10 / 0-13	23-29 / 0-F
	11-16 / 0-12	2A-2D / 0-E

**ALL VALUES ON THIS PAGE ARE HEX

Figure 6-6d. FD Controller Unclamp Command

■ Issued   ▤ Returned   FORMAT

6504	68000	DESCRIPTOR	RANGE	COMMENT
0000	FCC001	gobyte	81	RWTS, zeroed
0001	FCC003	function	03	format
0002	FCC005	drive	00, 80	00 = top
0003	FCC007	side	00, 01	00 = top
0004	FCC009	sector	00..15	see below*
0005	FCC00B	track	00..2D	beginning track #
0006	FCC00D	speed	DA..23	00 = norm, DA = fast
0007	FCC00F	confirm	FF	format confirmation
0008	FCC011	status	00..1C	00 = no error
0009	FCC013	dsk ID	00..02	00 duo, 01 lisa, 02 mac
002C	FCC059	retry	00..64	64 = no retrys
005B	FCC0B7	dat bitslp1	00..FF	00 = no error
005C	FCC0B9	dat bitslp2	00..FF	00 = no error
005D	FCC0BB	dat chksm	00..FF	00 = no error
005E	FCC0BD	adr bitslp1	00..01	00 = no error
005F	FCC0BF	adr bitslp2	00..FF	00 = no error
0060	FCC0C1	wrong sec	00..FF	00 = no error
0061	FCC0C3	wrong trk	00..01	00 = no error
0062	FCC0C5	adr chksm	00..FF	00 = no error
007E	FCC0FD	usr chksm	00..FF	user
007F	FCC0FF	usr chksm	00..FF	user
0080	FCC101	usr chksm	00..FF	user
01D0	FCC3A1	bad sec total	00..max sector	error only
01D1	FCC3A3	error trk #	00..max track	error only
01D2	FCC3A5	error side #	00, 01	error only
01D3	FCC3A7	bad sector map	00..max sector	error only
01F4	FCC3E9	buf begin		R/W data
03FF	FCC7FF	buf end		
COPS PB=4	FCDD81	FDIR	digital bit	high = interrupt pending
Parallel PB=6	FCC901	DSKDIAG	digital bit	low = busy

FCD

Pre issue requirements: drive enabled
                             DSKDIAG high
                             gobyte zeroed
                             no interrupts pending

Post issue memory access: none until FDIR

*
tracks/sectors	tracks/sectors
0-3 / 0-15	17-1C / 0-11
4-A / 0-14	1D-22 / 0-10
B-10 / 0-13	23-29 / 0-F
11-16 / 0-12	2A-2D / 0-E

**ALL VALUES ON THIS PAGE ARE HEX

Figure 6-6e. FD Controller Format Command

Issued	Returned	VERIFY		
6504	68000	DESCRIPTOR	RANGE	COMMENT
0000	FCC001	gobyte	81	RWTS, zeroed
0001	FCC003	function	04	verify
0002	FCC005	drive	00, 80	00 = top
0003	FCC007	side	00, 01	00 = top
0004	FCC009	sector	00..15	see below*
0005	FCC00B	track	00..2D	beginning track
0006	FCC00D	speed	DA..23	00 = norm, DA = fast
0007	FCC00F	confirm	FF	format confirmation
0008	FCC011	status	00..1C	00 = no error
0009	FCC013	dsk ID	00..02	00 duo, 01 lisa, 02 mac
002C	FCC059	retry	00..64	64 = no retrys
005B	FCC0B7	dat bitslp1	00..FF	00 = no error
005C	FCC0B9	dat bitslp2	00..FF	00 = no error
005D	FCC0BB	dat chksm	00..FF	00 = no error
005E	FCC0BD	adr bitslp1	00..FF 01	00 = no error
005F	FCC0BF	adr bitslp2	00..FF	00 = no error
0060	FCC0C1	wrong sec	00..FF	00 = no error
0061	FCC0C3	wrong trk	00..FF 01	00 = no error
0062	FCC0C5	adr chksm	00..FF	00 = no error
007E	FCC0FD	usr chksm	00..FF	user
007F	FCC0FF	usr chksm	00..FF	user
0080	FCC101	usr chksm	00..FF	user
01D0	FCC3A1	bad sec total	00..max sector	error only
01D1	FCC3A3	error trk #	00..max track	error only
01D2	FCC3A5	error side #	00, 01	error only
01D3	FCC3A7	bad sector map	00..max sector	error only
01F4	FCCSE9	buf begin	R/W data	
03FF	FCC7FF	buf end		
COPS PB=4	FCDD81	FDIR	digital bit	high = interrupt pending
Parallel PB=6 FCC901		DSKDIAG	digital bit	low = busy

FCD

Pre issue requirements:	drive enabled
	DSKDIAG high
	gobyte zeroed
	no interrupts pending
Post issue memory access:	none until FDIR

**	tracks/sectors	tracks/sectors
	0-3 / 0-15	17-1C / 0-11
	4-A / 0-14	1D-22 / 0-10
	B-10 / 0-13	23-29 / 0-F
	11-16 / 0-12	2A-2D / 0-E

**ALL VALUES ON THIS PAGE ARE HEX

Figure 6-6f. FD Controller Verify Command

6-18

Issued / Returned / FORMAT TRACK

6504	68000	DESCRIPTOR	RANGE	COMMENT
0000	FCC001	gobyte	81	RWTS, zeroed
0001	FCC003	function	05	format track
0002	FCC005	drive	00, 80	00 = top
0003	FCC007	side	00, 01	00 = top
0004	FCC009	sector	00..15	see below**
0005	FCC00B	track	00..2D	00 = outer
0006	FCC00D	speed	DA..23	00 = norm, DA = fast
0007	FCC00F	confirm	FF	format confirmation
0008	FCC011	status	00..1C	00 = no error
0009	FCC013	dsk ID	00..02	00 duo, 01 lisa, 02 mac
002C	FCC059	retry	00..64	64 = no retrys
005B	FCC0B7	dat bitslp1	00..FF	00 = no error
005C	FCC0B9	dat bitslp2	00..FF	00 = no error
005D	FCC0BB	dat chksm	00..FF	00 = no error
005E	FCC0BD	adr bitslp1	00..FF 01	00 = no error
005F	FCC0BF	adr bitslp2	00..FF	00 = no error
0060	FCC0C1	wrong sec	00..FF	00 = no error
0061	FCC0C3	wrong trk	00..FF 01	00 = no error
0062	FCC0C5	adr chksm	00..FF	00 = no error
007E	FCC0FD	usr chksm	00..FF	user
007F	FCC0FF	usr chksm	00..FF	user
0080	FCC101	usr chksm	00..FF	user
01D0	FCC3A1	bad sec total	00..max sector	error only
01D1	FCC3A3	error trk #	00..max track	error only
01D2	FCC3A5	error side #	00, 01	error only
01D3	FCC3A7	bad sector map	00..max sector	error only
01F4	FCC5E9	buf begin		R/W data
03FF	FCC7FF	buf end		
COPS PB=4	FCDD81	FDIR	digital bit	high = interrupt pending
Parallel PB=6	FCC901	DSKDIAG	digital bit	low = busy

FCD ___

Pre issue requirements: drive enabled
                                 DSKDIAG high
                                 gobyte zeroed
                                 no interrupts pending

Post issue memory access: none until FDIR

*	tracks/sectors	tracks/sectors
	0-3 / 0-15	17-1C / 0-11
	4-A / 0-14	1D-22 / 0-10
	B-10 / 0-13	23-29 / 0-F
	11-16 / 0-12	2A-2D / 0-E

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Figure 6-6g. FD Controller Format Track Command

6-19

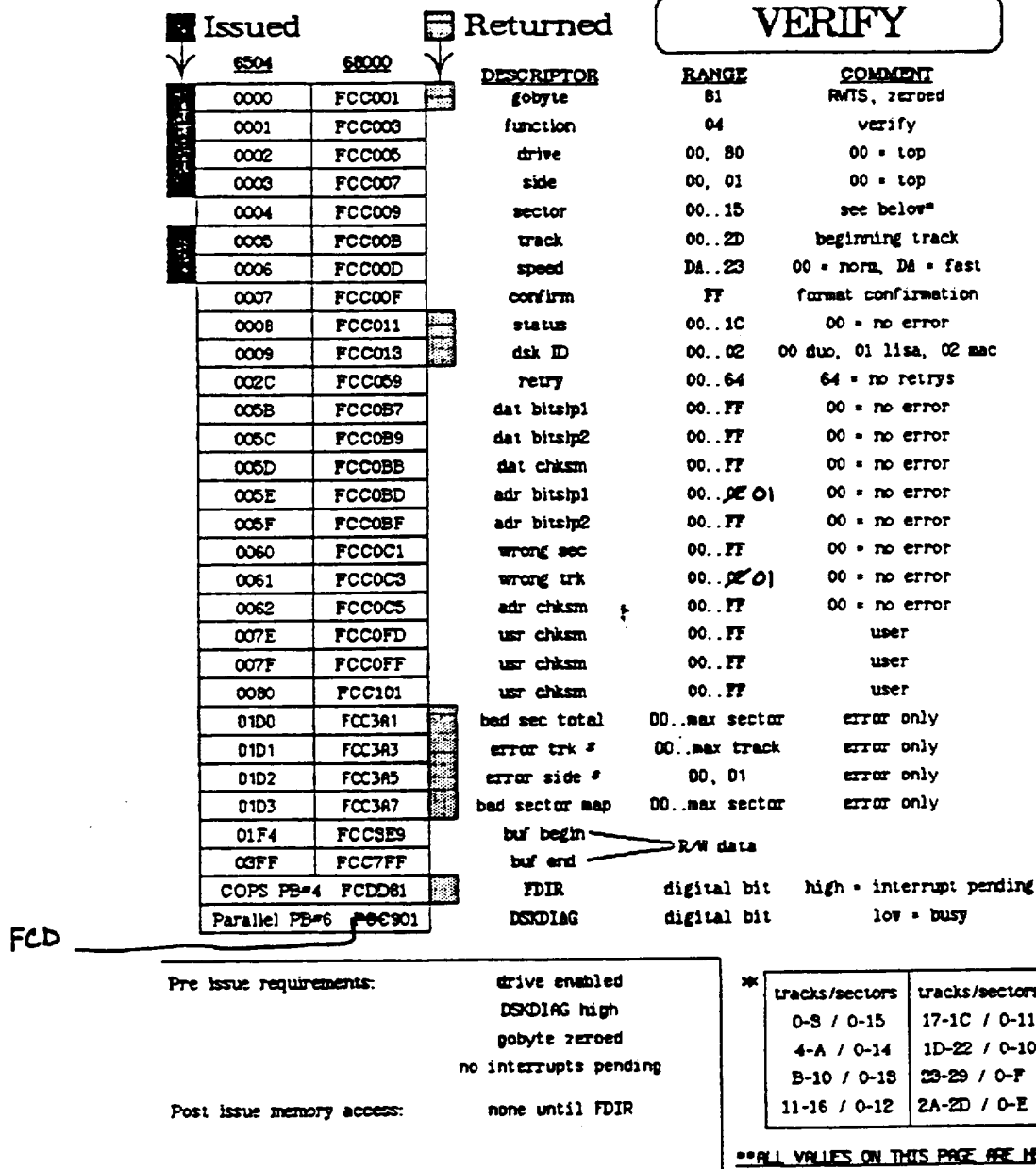September 7th 1982   LISA Hardware Manual

■ Issued   ⊟ Returned   (VERIFY TRACK)

6504	68000	DESCRIPTOR	RANGE	COMMENT
0000	FCC001	gobyte	81	RWTS, zeroed
0001	FCC003	function	06	verify track
0002	FCC005	drive	00, 80	00 = top
0003	FCC007	side	00, 01	00 = top
0004	FCC009	sector	00..15	see below*
0005	FCC00B	track	00..2D	00 = outer
0006	FCC00D	speed	DA..23	00 = norm, DA = fast
0007	FCC00F	confirm	FF	format confirmation
0008	FCC011	status	00..1C	00 = no error
0009	FCC013	disk ID	00..02	00 duo, 01 lisa, 02 mac
002C	FCC059	retry	00..64	64 = no retrys
005B	FCC0B7	dat bitslp1	00..FF	00 = no error
005C	FCC0B9	dat bitslp2	00..FF	00 = no error
005D	FCC0BB	dat chksm	00..FF	00 = no error
005E	FCC0BD	adr bitslp1	00..00 01	00 = no error
005F	FCC0BF	adr bitslp2	00..FF	00 = no error
0060	FCC0C1	wrong sec	00..FF	00 = no error
0061	FCC0C3	wrong trk	00..00 01	00 = no error
0062	FCC0C5	adr chksm	00..FF	00 = no error
007E	FCC0FD	usr chksm	00..FF	user
007F	FCC0FF	usr chksm	00..FF	user
0080	FCC101	usr chksm	00..FF	user
01D0	FCC3A1	bad sec total	00..max sector	error only
01D1	FCC3A3	error trk #	00..max track	error only
01D2	FCC3A5	error side #	00, 01	error only
01D3	FCC3A7	bad sector map	00..max sector	error only
01F4	FCC3E9	buf begin		R/W data
03FF	FCC7FF	buf end		
COPS PB=4 FCDD81		FDIR	digital bit	high = interrupt pending
Parallel PB=6 FCC901		DSKDIAG	digital bit	low = busy

FCD

Pre issue requirements: drive enabled
                               DSKDIAG high
                               gobyte zeroed
                               no interrupts pending

Post issue memory access: none until FDIR

**	tracks/sectors	tracks/sectors
	0-3 / 0-15	17-1C / 0-11
	4-A / 0-14	1D-22 / 0-10
	B-10 / 0-13	23-29 / 0-F
	11-16 / 0-12	2A-2D / 0-E

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Figure 6-6h. FD Controller Verify Track Command

6-20

■ Issued   ⊞ Returned   (READ brute force)

6504	68000	DESCRIPTOR	RANGE	COMMENT
0000	FCC001	gobyte	81	RWTS, zeroed
0001	FCC003	function	07	read (disregard checksum)
0002	FCC005	drive	00, 80	00 = top
0003	FCC007	side	00, 01	00 = top
0004	FCC009	sector	00..15	see below*
0005	FCC00B	track	00..2D	00 = outer
0006	FCC00D	speed	DA..23	00 = norm, DA = fast
0007	FCC00F	confirm	FF	format confirmation
0008	FCC011	status	00..1C	00 = no error
0009	FCC013	disk ID	00..02	00 duo, 01 lisa, 02 mac
002C	FCC059	retry	00..64	64 = no retrys
005B	FCC0B7	dat bitslp1	00..FF	00 = no error
005C	FCC0B9	dat bitslp2	00..FF	00 = no error
005D	FCC0BB	dat chksm	00..FF	00 = no error
005E	FCC0BD	adr bitslp1	00..02 01	00 = no error
005F	FCC0BF	adr bitslp2	00..FF	00 = no error
0060	FCC0C1	wrong sec	00..FF	00 = no error
0061	FCC0C3	wrong trk	00..02 01	00 = no error
0062	FCC0C5	adr chksm	00..FF	00 = no error
007E	FCC0FD	usr chksm	00..FF	user
007F	FCC0FF	usr chksm	00..FF	user
0080	FCC101	usr chksm	00..FF	user
01D0	FCC3A1	bad sec total	00..max sector	error only
01D1	FCC3A3	error trk #	00..max track	error only
01D2	FCC3A5	error side #	00, 01	error only
01D3	FCC3A7	bad sector map	00..max sector	error only
01F4	FCC3E9	buf begin	R/W data	
03FF	FCC7FF	buf end		
COPS PB=4	FCDD81	FDIR	digital bit	high = interrupt pending
Parallel PB=6	FC6901	DSKDIAG	digital bit	low = busy

FCD

Pre issue requirements: DSKDIAG high
                               drive enabled
                               gobyte zeroed
                               no interrupts pending

Post issue memory access: none until FDIR

*	tracks/sectors	tracks/sectors
	0-3 / 0-15	17-1C / 0-11
	4-A / 0-14	1D-22 / 0-10
	B-10 / 0-13	23-29 / 0-F
	11-16 / 0-12	2A-2D / 0-E

**ALL VALUES ON THIS PAGE ARE HEX

Figure 6-6i. FD Controller Read Brute Force Command

6-2_

Issued			Returned	WRITE brute force		
	6504	68000		DESCRIPTOR	RANGE	COMMENT
	0000	FCC001		gobyte	81	RWTS, zeroed
	0001	FCC003		function	08	write (user checksum)
	0002	FCC005		drive	00, 80	00 = top
	0003	FCC007		side	00, 01	00 = top
	0004	FCC009		sector	00..15	see below*
	0005	FCC00B		track	00..2D	00 = outer
	0006	FCC00D		speed	DA..23	00 = norm, DA = fast
	0007	FCC00F		confirm	FF	format confirmation
	0008	FCC011		status	00..1C	00 = no error
	0009	FCC013		disk ID	00..02	00 duo, 01 lisa, 02 mac
	002C	FCC059		retry	00..64	64 = no retrys
	005B	FCC0B7		dat bitslp1	00..FF	00 = no error
	005C	FCC0B9		dat bitslp2	00..FF	00 = no error
	005D	FCC0BB		dat chksm	00..FF	00 = no error
	005E	FCC0BD		adr bitslp1	00..01	00 = no error
	005F	FCC0BF		adr bitslp2	00..FF	00 = no error
	0060	FCC0C1		wrong sec	00..FF	00 = no error
	0061	FCC0C3		wrong trk	00..01	00 = no error
	0062	FCC0C5		adr chksm	00..FF	00 = no error
	007E	FCC0FD		usr chksm	00..FF	user
	007F	FCC0FF		usr chksm	00..FF	user
	0080	FCC101		usr chksm	00..FF	user
	01D0	FCC3A1		bad sec total	00..max sector	error only
	01D1	FCC3A3		error trk #	00..max track	error only
	01D2	FCC3A5		error side #	00, 01	error only
	01D3	FCC3A7		bad sector map	00..max sector	error only
	01F4	FCC3E9		buf begin	R/W data	
	03FF	FCC7FF		buf end		
	COPS PB=4	FCDD81		FDIR	digital bit	high = interrupt pending
	Parallel PB=6	FCE901		DSKDIAG	digital bit	low = busy

FCD

Pre issue requirements:	DSKDIAG high
	drive enabled
	gobyte zeroed
	no interrupts pending
Post issue memory access:	none until FDIR

*	tracks/sectors	tracks/sectors
	0-3 / 0-15	17-1C / 0-11
	4-A / 0-14	1D-22 / 0-10
	B-10 / 0-13	23-29 / 0-F
	11-16 / 0-12	2A-2D / 0-E

**ALL VALUES ON THIS PAGE ARE HEX

Figure 6-6j. FD Controller Write Brute Force Command

6-22

■ Issued   ▤ Returned   ┌─────────────┐
                                      │   CLAMP   │
                                      └─────────────┘

6504	68000	DESCRIPTOR	RANGE	COMMENT
0000	FCC001	gobyte	81	RWTS, zeroed
0001	FCC003	function	09	clamp
0002	FCC005	drive	00, 80	00 = top
0003	FCC007	side	00, 01	00 = top
0004	FCC009	sector	00..15	see below*
0005	FCC00B	track	00..2D	00 = outer
0006	FCC00D	speed	DA..23	00 = norm, DA = fast
0007	FCC00F	confirm	FF	format confirmation
0008	FCC011	status	00..1C	00 = no error
0009	FCC013	dsk ID	00..02	00 duo, 01 lisa, 02 mac
002C	FCC059	retry	00..64	64 = no retrys
005B	FCC0B7	dat bitslp1	00..FF	00 = no error
005C	FCC0B9	dat bitslp2	00..FF	00 = no error
005D	FCC0BB	dat chksm	00..FF	00 = no error
005E	FCC0BD	adr bitslp1	00..FF 01	00 = no error
005F	FCC0BF	adr bitslp2	00..FF	00 = no error
0060	FCC0C1	wrong sec	00..FF	00 = no error
0061	FCC0C3	wrong trk	00..FF 01	00 = no error
0062	FCC0C5	adr chksm	00..FF	00 = no error
007E	FCC0FD	usr chksm	00..FF	user
007F	FCC0FF	usr chksm	00..FF	user
0080	FCC101	usr chksm	00..FF	user
01D0	FCC3A1	bad sec total	00..max sector	error only
01D1	FCC3A3	error trk #	00..max track	error only
01D2	FCC3A5	error side #	00, 01	error only
01D3	FCC3A7	bad sector map	00..max sector	error only
01F4	FCC3E9	buf begin		R/W data
03FF	FCC7FF	buf end		
COPS PB#4	FCDD81	FDIR	digital bit	high = interrupt pending
Parallel PB#6	FCE901	DSKDIAG	digital bit	low = busy

FCD

Pre issue requirements: DSKDIAG high
                              drive enabled
                              gobyte zeroed
                              no interrupts pending

Post issue memory access: none until FDIR

*	tracks/sectors	tracks/sectors
	0-3 / 0-15	17-1C / 0-11
	4-A / 0-14	1D-22 / 0-10
	B-10 / 0-13	23-29 / 0-F
	11-16 / 0-12	2A-2D / 0-E

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Figure 6-6k. FD Controller Clamp Command

6-23

■ Issued   ▤ Returned   ┌─────────────┐
                                              │   SEEK   │
  6504   68000   └─────────────┘

6504	68000	DESCRIPTOR	RANGE	COMMENT
0000	FCC001	gobyte	83	SEEK, zeroed
0001	FCC003	function	00	
0002	FCC005	drive	00, 80	00 = top
0003	FCC007	side	00, 01	00 = top
0004	FCC009	sector	00..15	see below*
0005	FCC00B	track	00..2D	00 = outer
0006	FCC00D	speed	DA..23	00 = norm, DA = fast
0007	FCC00F	confirm	FF	format confirmation
0008	FCC011	status	00..1C	00 = no error
0009	FCC013	dsk ID	00..02	00 duo, 01 lisa, 02 mac
002C	FCC059	retry	00..64	64 = no retrys
005B	FCC0B7	dat bitslp1	00..FF	00 = no error
005C	FCC0B9	dat bitslp2	00..FF	00 = no error
005D	FCC0BB	dat chksm	00..FF	00 = no error
005E	FCC0BD	adr bitslp1	00..FF 01	00 = no error
005F	FCC0BF	adr bitslp2	00..FF	00 = no error
0060	FCC0C1	wrong sec	00..FF	00 = no error
0061	FCC0C3	wrong trk	00..FF 01	00 = no error
0062	FCC0C5	adr chksm	00..FF	00 = no error
007E	FCC0FD	usr chksm	00..FF	user
007F	FCC0FF	usr chksm	00..FF	user
0080	FCC101	usr chksm	00..FF	user
01D0	FCC3A1	bad sec total	00..max sector	error only
01D1	FCC3A3	error trk #	00..max track	error only
01D2	FCC3A5	error side #	00, 01	error only
01D3	FCC3A7	bad sector map	00..max sector	error only
01F4	FCC3E9	buf begin		R/W data
03FF	FCC7FF	buf end		
COPS PB#4	FCDD81	FDIR	digital bit	high = interrupt pending
Parallel PB#6	FCC901	DSKDIAG	digital bit	low = busy

FCD

Pre issue requirements: DSKDIAG high
                               gobyte zeroed

Post issue memory access: no special requirements
                             gobyte zeroed after command validation

*
tracks/sectors	tracks/sectors
0-3 / 0-15	17-1C / 0-11
4-A / 0-14	1D-22 / 0-10
B-10 / 0-13	23-29 / 0-F
11-16 / 0-12	2A-2D / 0-E

**ALL VALUES ON THIS PAGE ARE HEX

Figure 6-61. FD Controller Seek Command

6-2

September 7th 1982   LISA Hardware Manual

■ Issued   ⊟ Returned   ⌈ CALL USER PROG ⌉
    6504   68000

6504	68000	DESCRIPTOR	RANGE	COMMENT
0000	FCC001	gobyte	84	CALL, zeroed
0001	FCC003	low address	00..FF	call address
0002	FCC005	high address	00..3F	call address
0003	FCC007	side	00, 01	00 = top
0004	FCC009	sector	00..15	see below*
0005	FCC00B	track	00..2D	00 = outer
0006	FCC00D	speed	DA..23	00 = norm, DA = fast
0007	FCC00F	confirm	FF	format confirmation
0008	FCC011	status	00..1C	00 = no error
0009	FCC013	dsk ID	00..02	00 duo, 01 lisa, 02 mac
002C	FCC059	retry	00..64	64 = no retrys
005B	FCC0B7	dat bits\p1	00..FF	00 = no error
005C	FCC0B9	dat bits\p2	00..FF	00 = no error
005D	FCC0BB	dat chksm	00..FF	00 = no error
005E	FCC0BD	adr bits\p1	00..FF 01	00 = no error
005F	FCC0BF	adr bits\p2	00..FF	00 = no error
0060	FCC0C1	wrong sec	00..FF	00 = no error
0061	FCC0C3	wrong trk	00..FF 01	00 = no error
0062	FCC0C5	adr chksm	00..FF	00 = no error
007E	FCC0FD	usr chksm	00..FF	user
007F	FCC0FF	usr chksm	00..FF	user
0080	FCC101	usr chksm	00..FF	user
01D0	FCC3A1	bad sec total	00..max sector	error only
01D1	FCC3A3	error trk #	00..max track	error only
01D2	FCC3A5	error side #	00, 01	error only
01D3	FCC3A7	bad sector map	00..max sector	error only
01F4	FCC3E9	buf begin		R/W data
03FF	FCC7FF	buf end		
COPS PB#4	FCDD81	FDIR	digital bit	high = interrupt pending
Parallel PB#6	FCC901	DSKDIAG	digital bit	low = busy

FCD

Pre issue requirements: DSKDIAG high
                               gobyte zeroed

Post issue memory access: no special requirements
                             gobyte zeroed after head park

** | tracks/sectors | tracks/sectors |
    |---------------|---------------|
    | 0-3 / 0-15 | 17-1C / 0-11 |
    | 4-A / 0-14 | 1D-22 / 0-10 |
    | B-10 / 0-13 | 23-29 / 0-F |
    | 11-16 / 0-12 | 2A-2D / 0-E |

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Figure 6-6m. FD Controller Call User Program Command

6-2C

■ Issued   ▤ Returned   CLEAR INT STAT

6504	68000	DESCRIPTOR	RANGE	COMMENT
0000	FCC001	gobyte	65	CLEAR INTERRUPTS, zeroed
0001	FCC003	mask	00..XAAAXBBB	X = dont care, B = top dr
0002	FCC005	drive	00, 80	00 = top
0003	FCC007	side	00, 01	00 = top
0004	FCC009	sector	00..15	see below
0005	FCC00B	track	00..2D	00 = outer
0006	FCC00D	speed	DA..23	00 = norm, DA = fast
0007	FCC00F	confirm	FF	format confirmation
0008	FCC011	status	00..1C	00 = no error
0009	FCC013	disk ID	00..02	00 duo, 01 lisa, 02 mac
002C	FCC059	retry	00..64	64 = no retrys
005B	FCC0B7	dat bitslp1	00..FF	00 = no error
005C	FCC0B9	dat bitslp2	00..FF	00 = no error
005D	FCC0BB	dat chksm	00..FF	00 = no error
005E	FCC0BD	adr bitslp1	00..FF 01	00 = no error
005F	FCC0BF	adr bitslp2	00..FF	00 = no error
0060	FCC0C1	wrong sec	00..FF	00 = no error
0061	FCC0C3	wrong trk	00..FF 01	00 = no error
0062	FCC0C5	adr chksm	00..FF	00 = no error
007E	FCC0FD	usr chksm	00..FF	user
007F	FCC0FF	usr chksm	00..FF	user
0080	FCC101	usr chksm	00..FF	user
01D0	FCC3A1	bad sec total	00..max sector	error only
01D1	FCC3A3	error trk #	00..max track	error only
01D2	FCC3A5	error side #	00, 01	error only
01D3	FCC3A7	bad sector map	00..max sector	error only
01F4	FCC3E9	buf begin		R/W data
03FF	FCC7FF	buf end		
COPS PB=4	FCDD81	FDIR	digital bit	high = interrupt pending
Parallel PB=6	FCC901	DSKDIAG	digital bit	low = busy

FCD

**ALL VALUES ON THIS PAGE ARE HEX

Pre issue requirements: DSKDIAG high
                              gobyte zeroed

Post issue memory access: no special requirements
gobyte zeroed after completion and error status update

bottom drv		MASK		top drv		
drs	rut1	but1	dip	drs	rut1	but1	dip

tracks/sectors	tracks/sectors
0-3 / 0-15	17-1C / 0-11
4-A / 0-14	1D-22 / 0-10
B-10 / 0-13	23-29 / 0-F
11-16 / 0-12	2A-2D / 0-E

Figure 6-6n FD Controller Clear Interrupt Status Command

6-ェ

■ Issued   ▣ Returned | DRIVE ENABLE |

6504	68000	DESCRIPTOR	RANGE	COMMENT
0000	FCC001	gobyte	B6	DRIVE INT ENABLE, zeroed
0001	FCC003	mask	00..AXXXBXXX	X = dont care, B = top
0002	FCC005	drive	00, 80	00 = top
0003	FCC007	side	00, 01	00 = top
0004	FCC009	sector	00..15	see below*
0005	FCC00B	track	00..2D	00 = outer
0006	FCC00D	speed	DA..23	00 = norm, DA = fast
0007	FCC00F	confirm	FF	
0008	FCC011	status	00..1C	00 = no error
0009	FCC013	dsk ID	00..02	00 duo, 01 lisa, 02 mac
002C	FCC059	retry	00..64	64 = no retrys
005B	FCC0B7	dat bitslp1	00..FF	00 = no error
005C	FCC0B9	dat bitslp2	00..FF	00 = no error
005D	FCC0BB	dat chksm	00..FF	00 = no error
005E	FCC0BD	adr bitslp1	00..0E01	00 = no error
005F	FCC0BF	adr bitslp2	00..FF	00 = no error
0060	FCC0C1	wrong sec	00..FF	00 = no error
0061	FCC0C3	wrong trk	00..0E01	00 = no error
0062	FCC0C5	adr chksm	00..FF	00 = no error
007E	FCC0FD	usr chksm	00..FF	user
007F	FCC0FF	usr chksm	00..FF	user
0080	FCC101	usr chksm	00..FF	user
01D0	FCC3A1	bad sec total	00..max sector	error only
01D1	FCC3A3	error trk #	00..max track	error only
01D2	FCC3A5	error side #	00, 01	error only
01D3	FCC3A7	bad sector map	00..max sector	error only
01F4	FCC3E9	buf begin	R/W data	
03FF	FCC7FF	buf end	R/W data	
COPS PB#4	FCDD81	FDIR	digital bit	high = interrupt pending
Parallel PB#6	FCC901	DSKDIAG	digital bit	low = busy

FCD

Pre issue requirements: DSKDIAG high
                            gobyte zeroed

Post issue memory access: no special requirements
    gobyte zeroed after completion and error status update

** tracks/sectors	tracks/sectors
0-3 / 0-15	17-1C / 0-11
4-A / 0-14	1D-22 / 0-10
B-10 / 0-13	23-29 / 0-F
11-16 / 0-12	2A-2D / 0-E

**ALL VALUES ON THIS PAGE ARE HEX

Figure 6-60. FD Controller Drive Enable Command

6-27

September 7th 1982   LISA Hardware Manual

■ Issued   ▤ Returned | DRIVE DISABLE |

6504	68000	DESCRIPTOR	RANGE	COMMENT
0000	FCC001	gobyte	87	DRIVE INT DISABLE, zeroed
0001	FCC003	mask	00..AXXXBXXX	X = dont care, B = top
0002	FCC005	drive	00, 80	00 = top
0003	FCC007	side	00, 01	00 = top
0004	FCC009	sector	00..15	see below*
0005	FCC00B	track	00..2D	00 = outer
0006	FCC00D	speed	DA..23	00 = norm, DA = fast
0007	FCC00F	confirm	FF	format confirmation
0008	FCC011	status	00..1C	00 = no error
0009	FCC013	dsk ID	00..02	00 duo, 01 lisa, 02 mac
002C	FCC059	retry	00..64	64 = no retrys
005B	FCC0B7	dat bitslp1	00..FF	00 = no error
005C	FCC0B9	dat bitslp2	00..FF	00 = no error
005D	FCC0BB	dat chksm	00..FF	00 = no error
005E	FCC0BD	adr bitslp1	00..2F01	00 = no error
005F	FCC0BF	adr bitslp2	00..FF	00 = no error
0060	FCC0C1	wrong sec	00..FF	00 = no error
0061	FCC0C3	wrong trk	00..2F01	00 = no error
0062	FCC0C5	adr chksm	00..FF	00 = no error
007E	FCC0FD	usr chksm	00..FF	user
007F	FCC0FF	usr chksm	00..FF	user
0080	FCC101	usr chksm	00..FF	user
01D0	FCC3A1	bad sec total	00..max sector	error only
01D1	FCC3A3	error trk #	00..max track	error only
01D2	FCC3A5	error side #	00, 01	error only
01D3	FCC3A7	bad sector map	00..max sector	error only
01F4	FCC3E9	buf begin		R/W data
03FF	FCC7FF	buf end		
COPS PB=4	FCDD81	FDIR	digital bit	high = interrupt pending
Parallel PB=6	FCC901	DSKDIAG	digital bit	low = busy

FCD

Pre issue requirements: DSKDIAG high
                               gobyte zeroed

Post issue memory access: no special requirements
    gobyte zeroed after completion and error status update

**
tracks/sectors	tracks/sectors
0-3 / 0-15	17-1C / 0-11
4-A / 0-14	1D-22 / 0-10
B-10 / 0-13	23-29 / 0-F
11-16 / 0-12	2A-2D / 0-E

**ALL VALUES ON THIS PAGE ARE HEX

Figure 6-6p. FD Controller Drive Disable Command

6-22

■ Issued　　　🗔 Returned　　　┌─ ROM WAIT ─┐

6504	68000	DESCRIPTOR	RANGE	COMMENT
0000	FCC001	gobyte	88	WAIT IN ROM UNTIL FLAGGED
0001	FCC003	function	00	
0002	FCC005	drive	00, 80	00 = top
0003	FCC007	side	00, 01	00 = top
0004	FCC009	sector	00..15	see below
0005	FCC00B	track	00..2D	00 = outer
0006	FCC00D	speed	D4..23	00 = norm, D4 = fast
0007	FCC00F	confirm	FF	format confirmation byte
0008	FCC011	status	00..1C	00 = no error
0009	FCC013	dsk ID	00..02	00 duo, 01 lisa, 02 mac
002C	FCC059	retry	00..64	64 = no retrys
005B	FCC0B7	dat bitslp1	00..FF	00 = no error
005C	FCC0B9	dat bitslp2	00..FF	00 = no error
005D	FCC0BB	dat chksm	00..FF	00 = no error
005E	FCC0BD	adr bitslp1	00..FF 01	00 = no error
005F	FCC0BF	adr bitslp2	00..FF	00 = no error
0060	FCC0C1	wrong sec	00..FF	00 = no error
0061	FCC0C3	wrong trk	00..FF 01	00 = no error
0062	FCC0C5	adr chksm	00..FF	00 = no error
007E	FCC0FD	usr chksm	00..FF	user
007F	FCC0FF	usr chksm	00..FF	user
0080	FCC101	usr chksm	00..FF	user
01D0	FCC3A1	bad sec total	00..max sector	error only
01D1	FCC3A3	error trk #	00..max track	error only
01D2	FCC3A5	error side #	00, 01	error only
01D3	FCC3A7	bad sector map	00..max sector	error only
01F4	FCC3E9	buf begin ─┐		
03FF	FCC7FF	buf end ─┴→ R/W data		
COPS PB=4	FCDD81	FDIR	digital bit	high = interrupt pending
Parallel PB=6	FC0901	DSKDIAG	digital bit	low = busy

FCD ─────

Pre issue requirements:	DSKDIAG high
	go byte zeroed

Post issue memory access:　　no special requirements
　　　　　　　　　　　gobyte zeroed after head park

6504 waits until 69, 96 sequence in gobyte

※
tracks/sectors	tracks/sectors
0-3 / 0-15	17-1C / 0-11
4-A / 0-14	1D-22 / 0-10
B-10 / 0-13	23-29 / 0-F
11-16 / 0-12	2A-2D / 0-E

**ALL VALUES ON THIS PAGE ARE HEX

Figure 6-6q. FD Controller ROM Wait Command

6-29

September 7th 1982   LISA Hardware Manual

	Issued			Returned		GO AWAY		

6504	68000	DESCRIPTOR	RANGE	COMMENT
0000	FCC001	gobyte	89	LOOP IN ROM PERMANTELY
0001	FCC003	function	00	
0002	FCC005	drive	00, 80	00 = top
0003	FCC007	side	00, 01	00 = top
0004	FCC009	sector	00..16	see below*
0005	FCC00B	track	00..2D	00 = outer
0006	FCC00D	speed	DA..23	00 = norm, DA = fast
0007	FCC00F	confirm	FF	format confirmation
0008	FCC011	status	00..1C	00 = no error
0009	FCC013	dsk ID	00..02	00 duo, 01 lisa, 02 mac
002C	FCC059	retry	00..64	64 = no retrys
005B	FCC0B7	dat bitslp1	00..FF	00 = no error
005C	FCC0B9	dat bitslp2	00..FF	00 = no error
005D	FCC0BB	dat chksm	00..FF	00 = no error
005E	FCC0BD	adr bitslp1	00..~~02~~ 01	00 = no error
005F	FCC0BF	adr bitslp2	00..FF	00 = no error
0060	FCC0C1	wrong sec	00..FF	00 = no error
0061	FCC0C3	wrong trk	00..~~02~~ 01	00 = no error
0062	FCC0C5	adr chksm	00..FF	00 = no error
007E	FCC0FD	usr chksm	00..FF	user
007F	FCC0FF	usr chksm	00..FF	user
0080	FCC101	usr chksm	00..FF	user
01D0	FCC3A1	bad sec total	00..max sector	error only
01D1	FCC3A3	error trk #	00..max track	error only
01D2	FCC3A5	error side #	00, 01	error only
01D3	FCC3A7	bad sector map	00..max sector	error only
01F4	FCC3E9	buf begin	R/W data	
03FF	FCC7FF	buf end		
COPS PB#4	PCDD81	FDIR	digital bit	high = interrupt pending
Parallel PB#6	~~P000901~~	DSKDIAG	digital bit	low = busy

FCD

Pre issue requirements: DSKDIAG high
                               gobyte zeroed

Post issue memory access: no special requirements

*	tracks/sectors	tracks/sectors
	0-3 / 0-15	17-1C / 0-11
	4-A / 0-14	1D-22 / 0-10
	B-10 / 0-13	23-29 / 0-F
	11-16 / 0-12	2A-2D / 0-E

**ALL VALUES ON THIS PAGE ARE HEX

Figure 6-6r. FD Controller Go Away Command

6-30

Execution of the macro commands received from the
CPU are under the control of the 6504. Upon
completion of the operation, the status of the
controller is available in the I/O control block for
interrogation by the CPU. Figure 6-7 shows the
general flow of macro command transfer and
execution.

Figure 6-7. Floppy-Disk Macro Command Flowchart
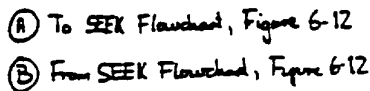
Figure 6-7. FD Macro Command Flowchart

6-31b

6.3.1 Disk Processor Operation

The 6504 processor executes code from the local ROM
storage within the floppy-disk controller. It is
routed to the routines contained therein on the
basis of the macro command placed in the I/O control
block of the local RAM by the 68000.

The 6504 is also responsible for the encoding and
decoding of the data for transfer to and from the
floppy-disk drive. The command RAM available to the
6504 is logically divided as shown in Figure 6-8.

Figure 6-8. Floppy-Disk Controller I/O Block

The floppy-disk controller RAM is shown in detail in
Figure 6-3. The read/write shared RAM is
initialized by the 6504 at power-on time. The
status block is used by the 6504 to indicate the
result of execution of a macro command. The
internal I/O block is used by the 6504 for internal
flags indicating progress in execution of an
operation. Variables used by the 6504 include both
local and variable intermixed. The parameter
storage is a space available to the 68000 and is not
accessed by the 6504. The 6504 stack fills the
space assigned to it from the high-order position
downwards. The I/O Buffer is a space of 524 bytes
used to transfer data between the floppy disk and
the 68000.

In order to proceed with disk operations, the 6504
inhibits interruption by the 68000. This enables
the timing routines that are performed by the 6504

0000	GO BYTE		
0001	COMMAND	ADR(L)	MASK
0002	DRIVE	ADR(H)	
0003	SIDE		
0004	SECTOR		
0005	TRACK		
0006	SPEED		
0007	FORMAT CONFIRM		
0008	ERRSTAT		
0009	DISK ID (0,1 or 2)		
000A ⋮ 000F	Reserved for Future Use.		

Figure 6-8. FD Controller I/O Block

6-32b

to be performed in real time until the operation is
complete and termination status is available to be
interrogated by the 68ØØØ.

The 65Ø4 firmware always executes in one of three
possible states:

  * Waiting for a macro command from the 68ØØØ
  * Checking the status of the drives
  * Executing a macro command.

When the controller is waiting for a command, the
65Ø4 uses a three-byte counter to control how long
the motors are left on after the last macro command
executed.

When the two low-order bytes decrement to zero, the
status of the disk is checked. This occurs about
once per second. The high byte of the counter is
directly modifiable by the 68ØØØ.

After disk status has been checked, the GOBYTE is
examined to see if a macro command has been loaded
and is awaiting execution. If the high-order bit is
set, for example, if the GOBYTE contains a negative
number, this indicates a command waiting. The
counter is decremented at approximately 1Ø
microsecond intervals. At a count of zero, the disk
drive motors are stopped.

The disk status is checked approximately once each
2/3 second. It is not checked more frequently
because the routine takes time and blocks any
response to the 68ØØØ while it is executing. It
also involves turning on the phiØ line to the disk
motor, which causes noise.

Both drives are checked for disk-in-place. Should
interrupts be enabled on a drive that changes this
status at this time, the 68ØØØ is interrupted to
inform it of the fact. The 68ØØØ must clear the
interrupt to issue the command that clamps the
disk. On a drive for which interrupts are not
enabled, the disk-in-place condition causes the disk
to be clamped automatically.

If the status shows the eject button was pushed,
nothing happens if no disk-in-place condition
exists. Otherwise, should interrupts be enabled, an
interrupt is sent to the 68ØØØ. If interrupts are
disabled, the disk is unclamped automatically.

6.3.2 Disk Macro Commands

The 6504 detects that the CPU has transmitted a
macro command to the floppy-disk controller by
monitoring the high-order bit of the GOBYTE in the
I/O block, 10B, for a 1 (one).

Upon detecting this, the first eight bytes of the
IOB are copied to the internal I/O block (IIOB).
Before any execution, interrupts are checked to see
if any are pending. If there are, the Clear
Interrupt Status command is allowed to execute.

The macro commands are divided into two classes,
depending on whether they do or do not interrupt the
68000 upon completion. Those that do interrupt
generally require extensive processing by the 6504
and the 68000 is locked out of shared memory for the
duration of instruction execution. Once the class
of the command has been determined, the GOBYTE is
cleared and the command parameters checked for
errors. If an error is detected the cause is placed
in the ERRSTAT byte and the command is aborted.

The macro commands that can be received follow. The
details of the commands and their associated
parameters are shown in Figure 6-6 above.

READ/WRITE DATA

Operations that involve an implied seek
operation. The I/O command block therefore
contains information on the desired drive, side,
track, and sector. The information returned to
the 68000 includes the status upon command
completion, a pointer to the buffer containing
data read, and a counter for the number of retries
that were required.

UNCLAMP

The operation that releases the disk currently
inserted in the drive so that it can be removed.
The input data states which drive, 00 or 80, and
the 68000 is interrupted by means of the FDIR
signal.

CLAMP

The operation that clamps a disk that has been
inserted in a drive for which interrupts are

enabled.

FORMAT and FORMAT TRACK

Operations that overwrite all data and markers on
the given track(s). They provide status
information, which includes the location of bad
sectors that could not be formatted correctly.

VERIFY and VERIFY TRACK

Operations that attempt to read track(s) and
inform the 68000 where errors are present in a
manner similar to the FORMAT. However, no write
operation is performed.

READ BRUTE FORCE (Ignore Checksum)

Identical to a READ operation, except that
agreement of the data with the three checksum
bytes written at the end of each sector is
ignored. It enables partly erroneous data to be
read.

WRITE BRUTE FORCE (User Checksum)

Identical to the WRITE operation, except that the
command supplies the three checksum bytes to be
written at the end of the sector. The controller
does not attempt to write the bytes that it would
normally generate. Ordinarily, data thus written
can only be read without error by a READ BRUTE
FORCE (Ignore Checksum) operation.

SEEK

The operation that moves the selected head to the
track required, but does not transfer any data.

CALL USER PROGRAM

The operation that initiates a routine that has
been down-loaded to the 6504 RAM area.

CLEAR INTERRUPT STATUS

The operation that clears the interrupt status to

the data output.

DRIVE ENABLE/DISABLE

The commands used to control the availabliity of
either of the two disk drives to the 68000.

ROM WAIT

The command that continually reads RAM, looking
for a two-byte sequence of 69 and 96. Once these
are found, the 6504 performs a cold start of the
6504. The purpose of this operation is primarily
to remove the 6504 from the RAM area while
diagnostics are being performed.

GO AWAY

The command that causes the 6504 to loop in ROM,
never accessing RAM or I/O. It is used to prevent
an erroneous WRITE operation to parameter memory
when the Lisa is turned off. Note that once
issued, this command cannot be stopped without
resetting the Lisa.

These operations result in a number of possible
status codes being returned to the 68000 via the
status byte, which indicates an error when it is
non-zero. In addition, error counters give the
number of occurrences of specific errors during the
performance of a given operation.

The floppy-disk controller attempts to retry an
operation on the disk, which results in an error
condition. This is attempted repeatedly until the
error count is exceeded. Retries involve moving the
head off track in increments of 1/8th of a track and
recalibrating the head using the optical sensor on
the drive.

The meaning of the possible error codes and the
error counters is shown in Figure 6-9.

```
            ERROR CODES          SIGNIFICANCE
        _____

            Ø1 (hex)         Invalid Command
            Ø2               Invalid Drive
            Ø3               Invalid Sector
            Ø4               Invalid Side
            Ø5               Invalid Track
            Ø6               Invalid Clear Mask
            Ø7               No Disk
            Ø8               Drive Not Enabled
            Ø9               Interrupts Pending
            ØA               Invalid Format Confirmation
            ØB               ROM Selftest Failure
            ØC               Unexpected IRQ or NMI

            14               Write Protect Error
            15               Unable to Verify
            16               Unable to Clamp
            17               Unable to Read
            18               Unable to Write
            19               Unable to Unclamp
            1A               Unable to Find Calibration
            1B               Unable to Adjust Speed
            1C               Unable to Write Calibration


     ERROR COUNTER ADDRESS    SIGNIFICANCE
        _____

            ØØ5B   (hex)     Bitslip Error Count
                             (data field start header)
            ØØ5C             Bitslip Error Count
                             (data field trailer)
            ØØ5D             Checksum Error Count
            ØØ5E             Bitslip Error Count
                             (ID field start header)
            ØØ5F             Bitslip Error Count
                             (ID field trailer)
            ØØ6Ø             Wrong Sector
            ØØ61             Wrong Track
            ØØ62             Header Checksum Error
```

Figure 6-9. Floppy-Disk Controller Error Codes

6.3.3 Data Encoding/Decoding

Data transferred to the floppy-disk controller by
the 68ØØØ for storage on the drives is not written
directly onto the disk. The data are encoded in the

following manner before it is stored:

* Three 8-bit bytes become four encoded
  bytes,
* The MSB of each encoded byte on the disk
  begins with a one,
* No more than two zero bits occur
  consecutively.

The data are encoded under control of the 6504 after
it has been placed in the buffer by the 68000, as
shown in Figure 6-10.

_ ~ _μ # ₁

GCR Codeword Table

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	96	97	9A	9B	9D	9E	9F	A6	A7	AB	AC	AD	AE	AF	B2	B3
10	B4	B5	B6	B7	B9	BA	BB	BC	BD	BE	BF	CB	CD	CE	CF	D3
20	D6	D7	D9	DA	DB	DC	DD	DE	DF	E5	E6	E7	E9	EA	EB	EC
30	ED	EE	EF	F2	F3	F4	F5	F6	F7	F9	FA	FB	FC	FD	FE	FF

Figure 6-10. Floppy-Disk Data Encoding Scheme

The MSB of each encoded byte must be a one so the
drive state machine can identify byte boundaries
when the data are being read from disk. The
requirement that no more than two zeroes occur
consecutively permits data to be written without
intervening clock bits. Transitions from the data
bits themselves occur frequently enough to permit
the state machine to remain synchronized with the
data being read.

The data are encoded from groups of three 8-bit
bytes into four encoded bytes by a table lookup
operation. It so happens that within the 128
possible codings of the other seven bits written to
the disk within one byte, there are more than 64
codings that satisfy the requirement of no more than
two consecutive zeroes.

6.3.4 Disk Formatting

A number of codings that are not used in data
translation are used to indicate a number of special
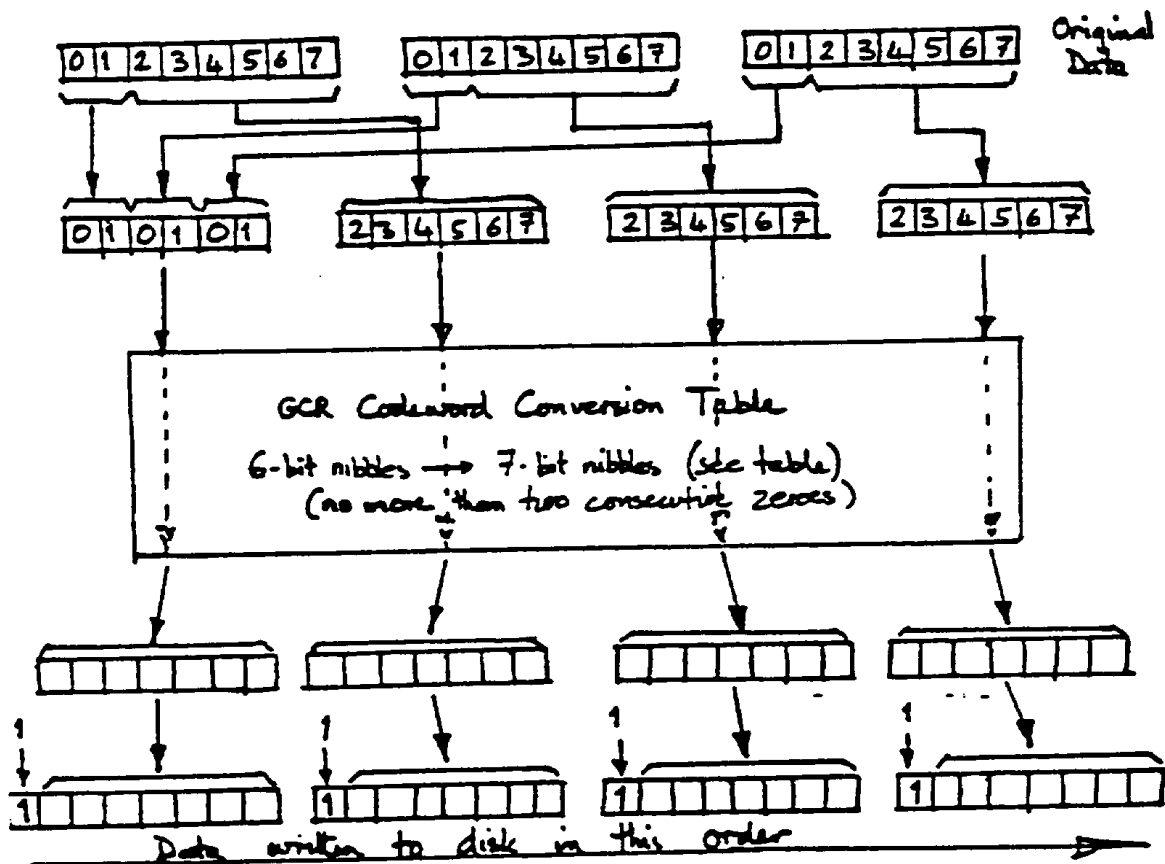
GCR Codeword Table

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	96	97	9A	9B	9D	9E	9F	A6	A7	AB	AC	AD	AE	AF	B2	B3
10	B4	B5	B6	B7	B9	BA	BB	BC	BD	BE	BF	CB	CD	CE	CF	D3
20	D6	D7	D9	DA	DB	DC	DD	DE	DF	E5	E6	E7	E9	EA	EB	EC
30	ED	EE	EF	F2	F3	F4	F5	F6	F7	F9	FA	FB	FC	FD	FE	FF

Figure 6-10.   FD Data Encoding Scheme
Floppy-Disk

6-38b

codes, such as headers within the format and speed
synchronization bytes.

The number of sectors and tracks are shown in Figure
6-11. Note that the number of sectors is dependent
on the track. This is due to the technique of
varying the rotational speed of the drive to allow
for the increased density possible on the outer
tracks of a disk.

→ ll #'s

Tracks	Sectors	r.p.m.	Speed Code
0-3	22	218.3	DC (hex)
4-10	21	228.7	CC
11-16	20	240.1	B8
17-22	19	252.7	A4
23-28	18	266.8	8E
29-34	17	282.5	75
35-41	16	300.1	59
42-45	15	320.1	38

Figure 6-11. Lisa Disk Format

Tracks 0 through 45 are normal data tracks. The
number of sectors contained on each track depends on
the track position as shown. This is due to
differing lengths of each track. The speed of disk
rotation is dynamically changed by the floppy-disk
controller to take advantage of this.

Track -1 is used as a speed synchronization track.
It is never written except during disk formatting.
The 6504 makes use of this track to adjust the speed
of rotation to within 0.4% of the desired speed.

Each sector is divided into four distinct fields, as
described below:

  * Header sync field
  * Header field
  * Data sync field
  * Data field.

HEADER SYNC FIELD

Contains a pattern of ones and zeroes that permits
the disk state machine to synchronize with the
data coming from disk. It consists of the
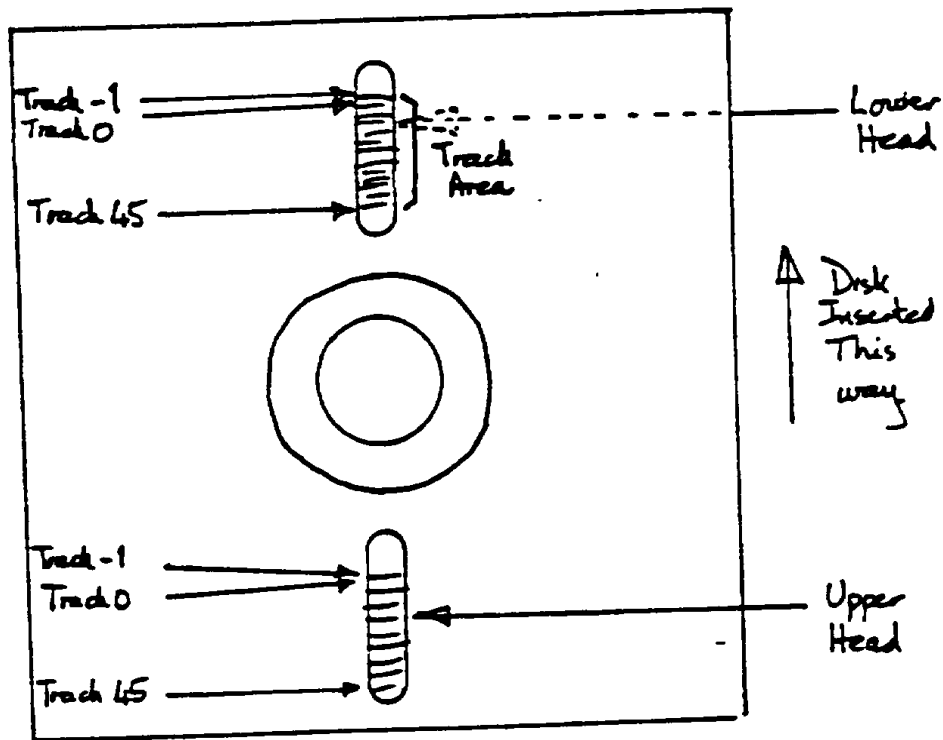
Tracks	Sectors	r.p.m.	Speed Code
0-3	22	218.3	DC (hex)
4-10	21	228.7	CC
11-16	20	240.1	B8
17-22	19	252.7	A4
23-28	18	266.8	8E
29-34	17	282.5	75
35-41	16	300.1	59
42-45	15	320.1	38

Figure 6-11. LISA Disk Format

6-29.5

following pattern:

                    32 "Self Synch" FFs
                    1Ø bytes A9 Speed Synchronization
                                    (only before Sector #Ø)

HEADER FIELD

    Uniquely identifies the sector on the disk, using
    the following pattern:

                D5   )
                AA   )   Header field identification
                96   )
                1 byte   TRACK identification number
                1 byte   SECTOR identification number
                1 byte   SIDE identification. ØØ or Ø1
                1 byte   VOLUME identification. May be one of
                          ØØ=AppleII or ///, Ø1=Lisa, Ø2=Mac
                1 byte   CHECKSUM coding. This is formed by
                          XOR'ing the previous four bytes
                DE   )
                AA   )   "Bit slip" marks
                1 byte   Pad byte where head is turned off

DATA SYNC FIELD

    Similar in purpose to the header sync field. It
    has the pattern:

                5 "Self Synch" FFs

DATA FIELD

    Contains the data written to the drive. Normally
    this is the only field written to except during a
    format operation. It has the pattern:

                D5   )
                AA   ) Data marks that identify a data field
                AD   )
                1 byte   Sector number
                524 bytes User data
                3 bytes   Checksum formed by adding data
                DE   )
                AA   )   "Bit slip" marks
                1 byte   Pad byte where head is turned off

    Note that the format is given in terms of the
    bytes handled by the 68ØØØ. The actual number of

bytes written to the disk is greater, since three
normal bytes map into four bytes on the disk, as
given by Figure 6-1Ø.

Self synch refers to a technique whereby two
zeroes are inserted between each synch byte
written to the disk. The state machine requires
no more than four self-synch fields, 8 ones and 2
zeroes, to synchronize its read operation with
disk rotation.

6.3.5 Disk State Machine Operation

The state machine that controls the flow of data
across the drive interface is shown in Figure 6-5
above.

There are five external inputs to the state
machine. These are the RDA, WRD, and SNS lines from
the disk, and the A2 and A3 control lines from the
control outputs of the LS259 shown at C-2 on sheet
4. The latter two are used to control the command
that the state machine is currently executing. The
four possible commands are:

* Sense
* Read
* Write
* Write Load.

In addition, there are two signals that are input to
the state machine ROM. These are the QA output of
the shift register, which provides the data stream
to be written to the disk, and the output of the
edge detector at D-1, which presents the data
transitions to the ROM as ones.

SPINDLE MOTOR SPEED CONTROL

During normal operation, the disk drive controls
the rotation by means of an integral speed control
circuit. When the drive performs a seek operation
outside of the current range of tracks, the speed
is adjusted according to the values given in
Figure 6-11. Disk speed is maintained to within
3% of that desired.

DRIVE REZERO and SEEK

Performed in a similar manner to ??? in that they both involve carriage motion. The four lines phi0-phi3 are manipulated to cause the carriage motor to step the required amount of tracks. In the case of a rezero, a sense operation determines whether the optical recalibration line is asserted to indicate that the carriage is at the known position of track -1.

Carriage movement is defined by the order in which the phi lines are manipulated. Thus a step through phi 3, 2, 1, and 0 moves the heads toward the calibration point, towards the front of the Lisa, by one half track. Stepping through 0, 1, 2, and 3 moves the heads away from the calibration point by one half track.

In order to minimize the positioning error from mechanical tolerances seeks are always completed by moving the carriage in the same direction, towards the calibration point, for the last half track, which is four increments. This means that seek direction is reversed during a seek away from the calibration point.

Carriage movement is performed in increments of 1/8th of a track. Allowance is made for head inertia by having three distinct time durations of each phi state before proceeding to the next. An example of a seek is shown in Figure 6-12.

Figure 6-12. Seek Flowchart

WRITE and WRITE LOAD

These commands operate together to provide the
write function to the drive. Each command
consists of 16 states in the state machine. Each
state is passed through in one clock cycle of 25Ø
ns.

Since the bit time on the disk is 2 microseconds,
the 16 states correspond to two bit times. The

Figure 6-12. Seek Flowchart

6-49b
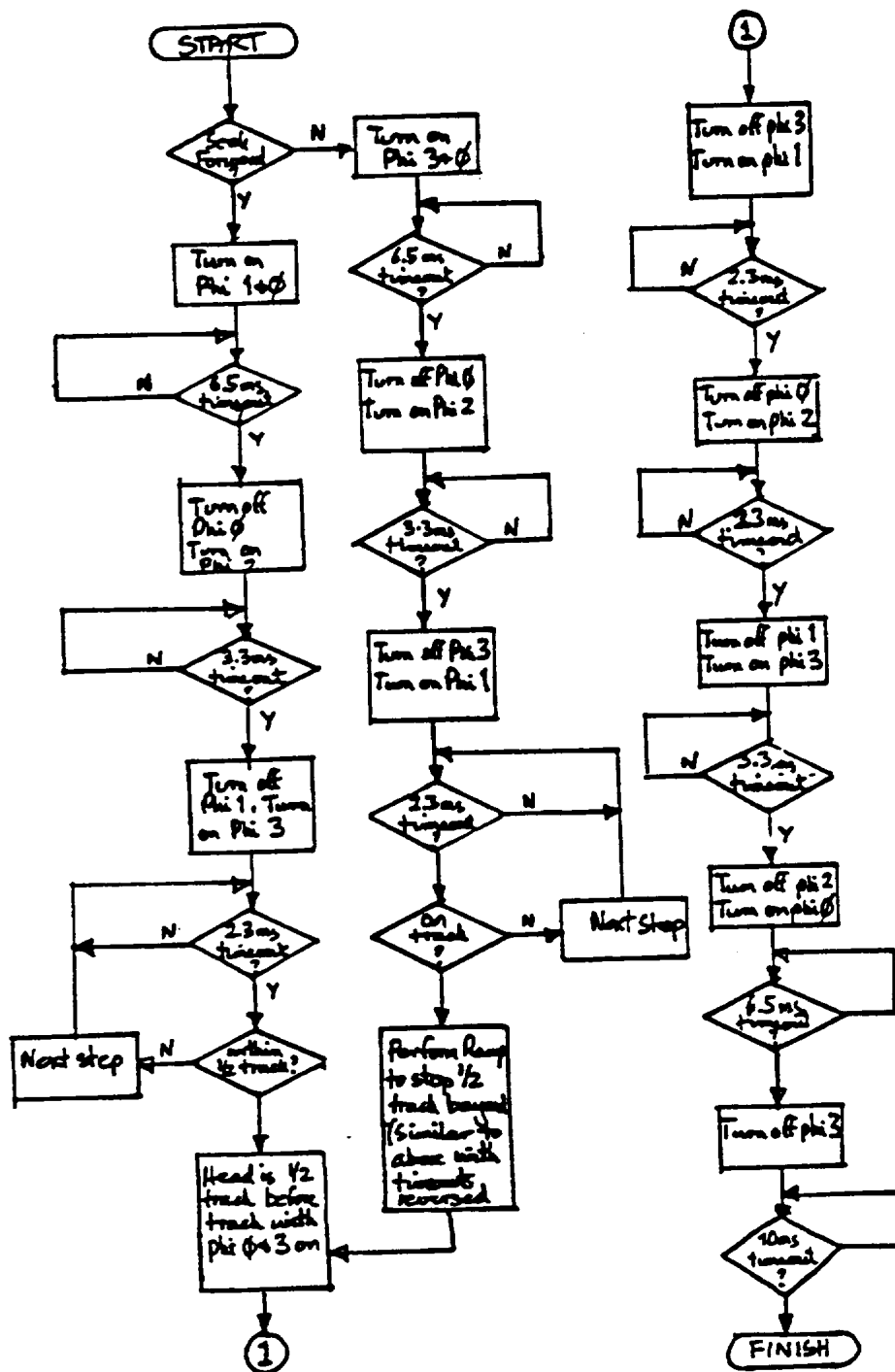
timing of the program loops in the 6504A is such
that exactly eight bit times occur between each
time that data are written to the shift register.
This write operation also causes the upper control
decoder to alter the A2 and A3 input configuration
to the ROM at D-2, which alters the state machine
into the Write Load command.

The state transitions in both the Write and Write
Load programs are designed so that that the WRD
signal is connected to the high-order state bit.
The QA output of the shift register thus controls
the data that is written to the disk.

READ

The read data are passed through two flops in
series to detect positive transitions. The format
of the Lisa floppy disks is such that no more than
two zero bits occur sequentially. The read
command shifts a one into the shift register when
a transition occurs and shifts in a zero when 2
microseconds pass without a transition.

It also attempts to hold the data in the shift
register for as long as possible when QA goes high
to indicate that an entire byte is correctly
aligned in the shift register. Following this,
the byte is transferred to RAM by the 6504, and
the state machine clears the shift register in
preparation for the next byte. Recall that all
bytes written to disk had a one in the MSB
position after data had been encoded.

SENSE

This is used to poll the status of the disk
drives. The HDS and phi0 lines are used to select
which of the four data bits are to be read
according to the following scheme:

HDS	phi0	Status Data
0	0	Write Protect
0	1	Optical Recalibration
1	0	Eject Button
1	1	Disk in Place

After the control lines have been configured to
sense the required data, the command is initiated

by setting the A2 and A3 inputs to 1@2. The MSB
of the shift register contains the sense bit. All
16 possible states in the sense command are
identical and cause a shift right operation.

6.4   The Serial I/O Controller

The I/O Board contains two serial interface ports, A and
B, that are controlled by a single serial I/O
controller. The software interface to this controller
is discussed in Chapter 2. The A-port conforms to the
RS232A specification; the B-port conforms to RS422.

The control logic is shown on the right side of sheet 3
of schematic Ø5Ø-4ØØ8. Refer to the block diagram of
the board in Figure 6-1 for a view of the hardware
context in which the serial controller operates.
Programming of the ports is discussed in subsection
3.5.1.

6.4.1 The Serial Port Controller

The serial ports are controlled by an 853Ø dual
serial-port controller. A discussion of the
controller can be found in the 853Ø user manual.

The controller connects to the internal I/O board D
bus. It is selected when the VMA signal coincides
with AS. The additional selection is performed on
the read and write inputs, which are derived from
the port decoding logic at B-3 on sheet 2.

The WSIO/ signal enables a write to the controller,
while an RSIO/ enables a read from it. These
signals originate in the controller decode logic at
A-3 on sheet 2. A configuration of address lines
A11-A9 of ØØ1 selects the serial-port controller.
The READ line distinguishes a read from a write.

The two low-order address bits of the system address
bus A1 and A2 are used to select between the two
ports and to define whether control information or
data are being transferred.

The PCLK device clock is derived from the 4 M, 4
MHz, clock signal at A-3 on sheet 2. This is in
turn derived from the 16 MHz clock from the
floppy-disk controller.

The controller interrupts the processor through the
RSIR/ signal on the system bus. Selection of
registers and functions within the controller is

made by means of the D/C/ and A/B/ pins. The first
indicates whether data or command information is
present on the bus lines. The second selects
between the A and B ports. Address lines A1 and A2
enable software to control this.

6.4.2 The Serial Ports

The two serial ports are provided in the form of two
25-pin DB connectors, as described in subsection
3.5.1.

The logic interface is shown on sheet 3 of the
schematics at A-1 through D-1. The signals that
correspond to port A are in the upper section of the
page and have signal names ending in "1." The signal
names and their function correspond to standard
RS232A nomenclature. The 1488 and 1489 devices
convert the TTL signals from the controller into the
+ or -12 V levels of the interface and vice-versa.

Port B signals are in the lower part of the page.
They provide an RS422-standard interface through use
of the 26LS3Ø and 26LS32 devices.

6.4.3 Baud Rate Generation

Selection of the baud rate used in either of the two
ports is performed internally by the 853Ø with the
aid of the 3.68 MHz oscillator between the SYNB and
TRXCB lines. Refer to the 853Ø user manual for
details on how baud rates are selected.

6.4.4 Serial Port Operation

The two serial ports operate independently of one
another. For details, refer to the serial-port
controller user manual.

6.5   Parallel Port Controller

The parallel port is used to interface a parallel
peripheral to the Lisa. A typical application is in the
attachment of an Apple ProFile hard disk drive.

The interface is discussed operationally in Chapter 2 of
this manual. The logic is shown on sheet 3 of schematic
Ø5Ø-4ØØ8.

The hardware consists of a 6522 I/O port device and some

associated logic. The 6522 is a 68ØØ-type peripheral
and is described in the 6522 data sheet.

6.5.1 68ØØØ Bus Interface for the Parallel-Port Controller

This is provided by the 6522. The I/O Board
internal D-bus connects to the data lines of the
6522, while addressing within the 16 locations
contained in the port controller is performed with
the system bus address lines A3 through A6.

Device selection is performed by having both the
DSKPT/ and VMA signals true. The former is provided
by the I/O decode at B-3 on sheet 1, while the
latter indicates that the processor is aware that it
is communicating with a 68ØØ-type device and has
modified the bus signals accordingly. Refer to the
68ØØØ user manual for a discussion of the VMA
signal.

The resulting address map for the port is shown in
Figures 2-11 and 2-12.

6522 reset is performed at the same time as Lisa
reset by means of the RESET/ signal at D-4, which
originates on the system bus.

The 6522 interrupts the 68ØØØ by means of the IOIR/
line, which is wired-ORed with the floppy-disk
controller interrupt (FDIR/) originating at B-1 on
sheet 4.

6522 clocking is performed by the E signal from the
system bus, which is connected to the phi2 input and
provides a 68ØØ-type compatible clock.

6.5.2 Parallel Port Interface

The 6522 provides two 8-bit ports, the A port and
the B port, for use in the interface itself. The A
port is used as the 8-bit parallel data interface,
while the B port is used for control lines.

The LS28Ø at D-3 is used to check parity as data are
being read from the interface into the Lisa. The
result of the check is latched in the LS1Ø9 JK flop
at D-3. The Reset input is presented as PRES/ to
the keyboard port at C-3 on sheet 2 to permit the
flip-flop to be reset. The Q output is on the
6522. The second LS28Ø at D-3 is used to generate
parity.

The lines on the B port are used as control and
status lines on the interface as follows:

BSY connects to PB1 and indicates to the 6522
that the interface is busy. It also connects
to CA1 to provide the data interrupt input.

Open Cable Detect (OCD) connects to the PB∅
line of the 6522. This signal is normally
held low at the peripheral end to signify
that the cable is connected. The Lisa
monitors this line and assumes that no
transfer can be performed when it is high.

The signal that is driven by PB2 is used as
an enable to the drivers' interface. When it
is low, both the LS245 8-bit data transceiver
and the LS244 control line drivers are
enabled.

DR/W/ is output from the PB3 line to the
peripheral as an indication of the direction
of data transfer. It is also used to define
the direction of the data transceiver's
drivers.

CMD/ is output to the peripheral from the PB4
line.

DSKDIAG is not input from the peripheral but
originates in the floppy-disk controller
section at B-1 on sheet 4. It indicates on
PB6 that the 68∅∅∅ is operating the interface
in diagnostic mode.

The port control lines of the 6522 are used as
follows:

CA1 is used to monitor the state of the BSY
line from the peripheral and to strobe the
data on the A port accordingly.

CA2 is used to provide the Peripheral Strobe
(PSTRB/) signal to the interface, which
indicates that either data are available for
a write or data has been received for a read
operation.

CB2 is used to monitor the parity status of
the interface.

6.5.3 Parallel Port Operation

Operation of the parallel port is under software
control and lies outside the scope of this manual.
Refer to software documentation and Chapter 2 of
this manual for programming information on this
port.

6.5.4 Parallel Port Timing

Timing on the parallel port is programmable and a
function of software. It therefore lies outside the
scope of this manual. Refer to the data sheet for a
discussion of the timing limitations on the 6522.

6.6   The Keyboard/Mouse Controller

The interface to the keyboard and the mouse is
implemented by means of a 6522 VIA peripheral port
device and a COPS single-chip controller. It is also
used to provide software control of the power on-off
function and to provide a real-time-clock.

Details on the 6522 can be found in the data sheet.
Refer to the COPS user manual for information on the
COPS. The logic that comprises the interface controller
is shown on sheet 2 of schematic $\emptyset5\emptyset$-4$\emptyset\emptyset$8 in Appendix
C. Programming of the controller is discussed in
subsection 2.5.4.

6.6.1 68$\emptyset\emptyset\emptyset$ Bus Interface for the Keyboard/Mouse Controller

This interface is implemented with the 6522. The
internal I/O board D-bus connects to the D$\emptyset$-D7 data
lines. Selection among the 16 internal register
destinations is performed by the A1 through A4
address lines from the system bus.

The device is selected when both the VMA signal on
the system bus and the I/O decode output at pin 7 of
device U4E are asserted. This indicates that the
processor board is performing an access to the
keyboard/mouse controller in a 68$\emptyset\emptyset$ compatible
cycle.

The address map of the controller as seen by the
software is shown in Figure 2-15.

The device is clocked by the E signal and reset by
the RESET/ line.

6.6.2 The COPS Processor

The COP421 shown at D-3 on sheet 2 is described in detail in the COPS user manual. As well as controlling data flow from the keyboard and mouse, the COP421 is responsible for maintaining the Time of Day clock. To do that it requires a power supply that is independent of the main supply; one that remains on even when the Lisa is turned off, as described in the next subsection.

The COPS connects to the A port of the 6522, with the CA1 and CA2 control signals of the 6522 being attached to the SO and SI lines of the COPS. In addition, the port PB6 control output signal connects with D3.

The other lines from the COPS are used as follows:

SK is the output to the keyboard. In conjunction with the D2 line, it is used to send a synchronization pulse to the keyboard to initiate data transfer.

G$\emptyset$ and G1 are the multiplexed data inputs from the keyboard and the mouse.

D1 and D2 are the select signals that are used to control the data multiplexer which provides keyboard and mouse data on G$\emptyset$ and G1.

D$\emptyset$ is used to switch the Lisa on and off under control of firmware resident in the COPS.

G2 is used to interrupt the processor by means of the NMI/ , non-maskable interrupt, at B-2 on sheet 2, which is presented to the processor board via the system bus, and to detect a power failure via D5 at B-2 on sheet 2.

G3 is used to sense the state of the on-off switch on the lower-left of the Lisa cabinet.

CK1 and CK2 are inputs to the COPS oscillator from timing circuit at D-2. The clock is crystal-controlled to permit the time of day to be kept accurately.

RST is the COPS internal reset input which is
used to perform a power-on reset in the COPS
should its own power have failed for any
reason.

6.6.3 Keyboard/Mouse Interface

Keyboard data are input on the KBD line. This line
is pulled low by the COPS generating a SYNC pulse to
signal the keyboard to send data if it has any.
This is done via the COPS SK output with the D2
output being asserted simultaneously.

The keyboard responds with an ACK pulse on the KBD
line, followed by a serial 8-bit byte which
indicates the code for a key pressed or released.
The keycodes are outlined in Figure 2-14. If no key
has changed its state, no ACK pulse is sent.

The mouse interface consists of the LS153 dual
4-to-1 multiplexer at D-2. The selection of data to
be input to the COPS is performed by configuring the
D1 and D2 outputs from the COPS.

The COPS polls the signal states by reading the
signals input to the mulitiplexer. The movement of
the mouse is detected by pulse edges on the relevant
direction lines. The three inputs SW∅-SW2 reflect
the state of up to three switches on the mouse. In
the current Lisa only one mouse switch is present
and is connected to the SW∅ line.

The data presented to the COPS is selected as shown
in Figure 6-13. Refer to Chapter 8 for a discussion
of the keyboard side of this interface.

Figure 6-13. Keyboard Data Format and Timing

6.6.4 Software On-Off/Reset Logic

The software on-off switch is sensed through the
PWRSW/ signal. In addition, pulling the RESET/
signal high when the Lisa is turned off pulls the
PWRSW/ signal low and turns the Lisa on. Note that
this can be also accomplished by pulling RESET/ to
+5STBY with a 1ØØ ohm resistor.

The COPS can turn the Lisa on or off, via the ON
line. The COPS may be programmed to turn the Lisa
on under control of the real-time-clock (RTC). The
RTC is not capable of turning the computer off.

6.6.5 Other Control Lines

The keyboard and mouse controller makes use of the A
port of the 6522. The B port is used to provide an
interface to the Lisa for several control lines that
would otherwise require additional hardware to
implement.

The use of the B port lines is as follows:

PBØ is used to reset the keyboard under
software control.
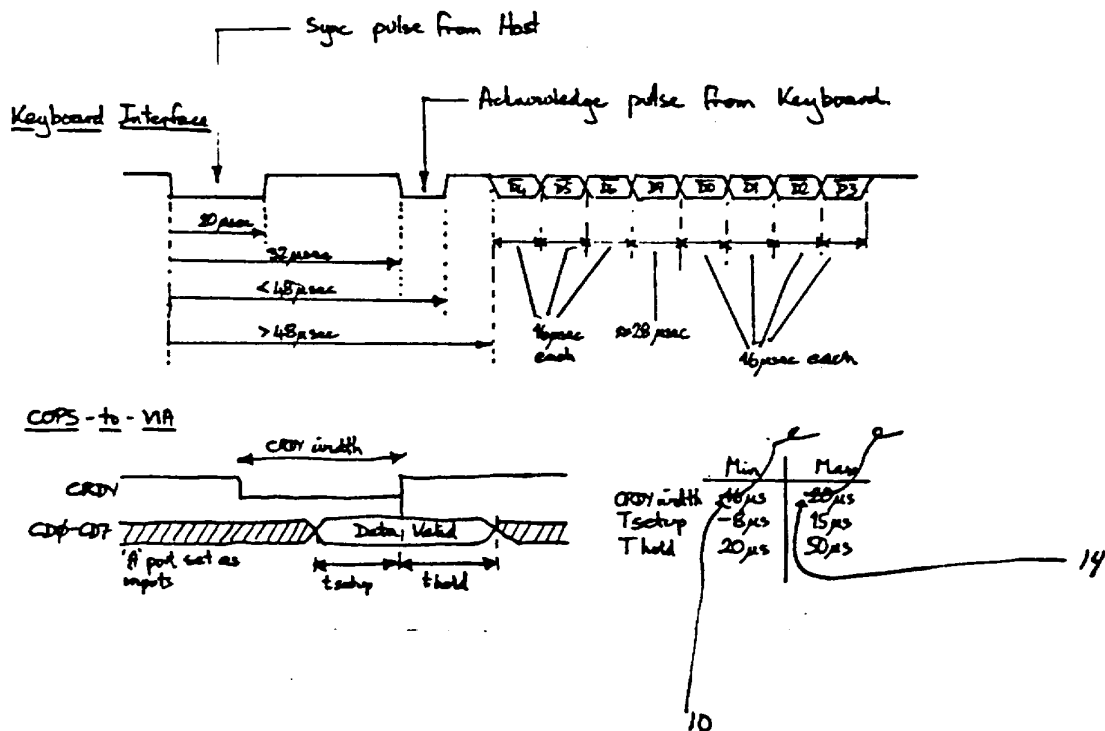
Figure 6-13. Keyboard Data Format and Timing

6-52b

PB1-PB3 are used for output of a digital
value to control the speaker volume.

PB4 is used to input the floppy-disk
interrupt (FDIR) status, which has been
latched by the floppy-disk processor in the
LS259 at B-1 on sheet 4.

PB5 is used to sense the PRES/ reset,
derived from the CRES/ bus signal at C-3.
The CRES/ signal is pulled low by RESET/ to
reset the parallel device. PB5 can be used
to reset a parity error on the parallel
interface at D-3 on sheet 3.

PB6 is used for the COPS handshake as
described above.

PB7 is used to output the CRES/ reset signal
to the parallel port interface at pin 117 of
the J1 connector.

6.7   Miscellaneous Logic

The I/O board contains several blocks of logic, which
have been located there for optimal use of board space
within the Lisa.

This section describes the hardware implementation of
the following functions:

* Speaker volume control
* Battery power control
* Video contrast latch.

6.7.1 Speaker Volume Control

The Lisa is equipped with a speaker; its volume can
be controlled by the software. The value of the
volume is presented by the PB1-PB3 lines of the
Keyboard 6522, and these are input to the D-to-A
ladder network shown at C-4 on sheet 5.

The resulting analog value is presented as a voltage
to pin 10 of device U10A. This operates as a
voltage follower to present a high input impedance
to the D-to-A ladder network.

The resulting output defines the speaker level,
while the TONE output from the 6522 defines the
frequency. The output signal is presented to pin 13
of A10, which drives the power transistors Q3 and Q4

to give the speaker output signal.

6.7.2 Battery Supply and Control

The Lisa is equipped with a battery located on the
I/O board. It provides a +5 V supply to operate the
COPS in the keyboard/mouse controller should the
Lisa be completely disconnected from a power source,
so that the Time-of-Day clock logic can continue to
function.

The battery automatically recharges itself when the
Lisa is on. The battery is capable of running the
COPS for 1∅ hours without loss of data. Once
battery power is exhausted, the battery supply shuts
down to avoid erratic COPS operation.

The circuit is shown at the bottom of sheet 5. It
is designed around the 4193 voltage regulator.
Recharge power for the batteries is provided by the
+12 VDC supply through diode D7. Zener D8 limits
the voltage output of the +5 V supply.

The 4193 operates by pulling the LX output to
ground, then allowing it to fly back up to produce
the output voltage. L1 is the flyback inductor,
while capacitor C12 smoothes the output.

The frequency with which the 4193 does this depends
on the voltage sensed by the LBR and VF inputs on
the precision voltage-divider formed by resistors
R19-R21. The VF input looks for a 1.3 V reference.
The voltage is higher than this when the +5 VSTBY
supply is operational, which supplies a level of
approximately 5.7 V. Allowing for a diode drop of
∅.3 V across D3 still results in the +5 V level
being pulled to over 5 V. At this time, the battery
is being recharged.

When the Lisa is disconnected from a power source,
the +5 STBY is removed and the +5 V level begins to
drop, which triggers the 4193 through the sensing
inputs from the ladder to attempt to restore the
level. The 4193 is capable of providing an
acceptable +5 V output for battery voltages as low
as +2.4 V.

The LBR input detects a 4.5 V level on the +5 V
output, and pulls the LBD output low. This resets
the flop formed by the two gates of CMOS device U14B
and pin 4 goes low. This forces Q6 to be
back-biased and disconnects the load from the
battery output. This is done to avoid cell

reversal, which can destroy nickel/cadmium battery
cells.

When the normal 5 V supply is operational, the pin
1Ø output of the inverter causes the flop to be held
off and transistor Q6 is always on.

6.7.3 Video Contrast Latch

This is shown in the upper part of sheet 5 of the
schematics. The data are input via the parallel
port interface 6522A port, which is latched in the
CMOS 74C174 at D-3. The data is presented to the
summing network, which presents the result of the
D-to-A conversion as a DC voltage to pin 3 of the
low-input-impedance voltage follower in the first
stage of device U1ØA.

The output of this is fed through R19 to the second
stage of device U1ØA, which functions as an
inverting amplifier with a gain of unity. The bias
network formed by resistors R1Ø and R11 provides a
bias voltage of approximately 3.5 V to pin 5. The
RESET signal pulls this point to ground, which
blanks the screen.

The CONT output can vary between +2 V, fully black,
and +7 V, fully white. This signal is an input to
the video board, which is described in Chapter 7.

CHAPTER 7. THE VIDEO BOARD

The video board provides most of the analog circuitry that
operates the Lisa's CRT. The board is mounted on the rear
wall of the CRT enclosure and contains hazardous voltages.
Extreme care should be taken when using the Lisa with the
video board exposed for troubleshooting.

The video digital control logic on the processor board drives
the video board. Refer to section 4.5 for a description of
the video control.

7.1   Block Diagram

To better describe the video board's operation, it has
been functionally divided into these major blocks:

* Power-supply circuits
* Video-amplifier circuits
* Vertical deflection circuits
* Horizontal deflection circuits.

The video board processes the bit stream of serial
display data it receives from the processor board and
translates the data into a display by means of the
raster scan on the screen. To perform this, signals
that synchronize the raster sweep with the data are also
provided by the processor board.

An overview of the video board is shown in Figure 7-1 as
a block diagram. This chapter refers to the video board
schematic, number 050-4012-A, in Appendix D.

Figure 7-1. Video Board Block Diagram

7.2   Power-Supply Circuits

Power is supplied to the video board via the connector
at the upper left of the schematic in Appendix D. The
+12 VDC is the same as that supplied to other circuits
in the Lisa. The +33 VDC is used exclusively by the
video board. Refer to Chapter 1∅ for a discussion of
the power supply and its capabilities.

Figure 7-1. Video Board Block Diagram

7-2b
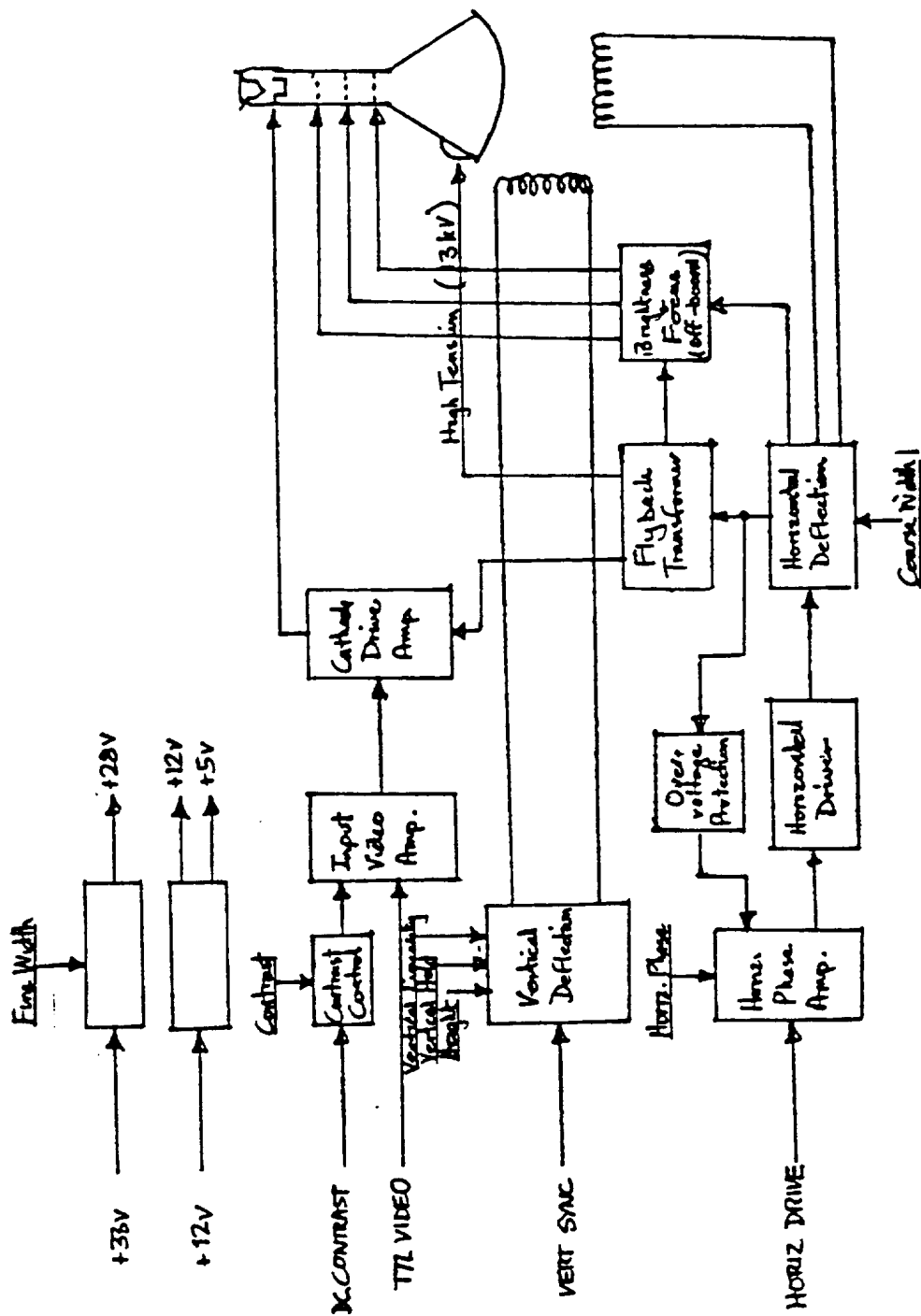
7.2.1 The +12 VDC and +5 VDC Supply

The +12 VDC input is a regulated voltage from the
power supply. It is applied to pin P of the
connector and is used to provide the following:

  * Power to the +5 VDC regulator
  * Power for the CRT filament
  * Collector supply to transistor Q8.

The +5 V regulator consists of the current-limiting
resistor R4, the 5.1 V zener diode CR1, and the
filter capacitor C3. This supply is used to provide
the collector supply of transistor Q7 and also to
provide base-bias for Q2. The current provided by
the +5 VDC supply is on the order of 3∅ milliamps.

7.2.2 The +33 VDC Supply

The +33 VDC input is an semi-regulated voltage
provided by the power supply. It is applied to pin
5 of the connector and is connected directly to the
24 V 3-terminal voltage regulator U1. The regulator
can accept voltages in the range +33 to +36 VDC and
continue to operate correctly. Voltages below about
+32 VDC prevent the regulator from performing
properly.

The reference terminal at pin 2 of U1 is biased
above ground by the resistor ladder formed by R1,
R2, and R3. Adjustment of the potentiometer R2
results in an output voltage at pin 3 which is 24 V
plus the DC voltage on pin 2. The normal voltage
range at pin 3 is between +26 and +3∅ VDC. The
function of this adjustment is to provide a fine
control of the width of the display on the CRT.

Capacitors C1 and C32 are provided to suppress
parasitic oscillations in the regulator. C2 acts as
a storage capacitor for the load.

The regulated +28 VDC, nominal, provided by the
supply provides power for the rest of the video
board and the CRT.

7.3 The Video-Amplifier Circuit

The function of the video-amplifier circuit is to take
the serial TTL data provided by the processor board and
convert the digital information into black, logical ∅,
or white, logical 1, pixels on the screen by controlling

the cathode emission in the CRT.

7.3.1 Video-Data Input and Contrast Control

TTL-level video data are presented to the video
board on pin 1 of the connector. It is impressed on
the base of transistor Q6 by way of the
current-limiting resistor R51. Resistors R51 and
R52 form a voltage-divider network to increase the
noise-rejection of Q6, which acts as a high-speed
switch. The collector of Q6 is therefore at ground
or at a DC level, depending on the digital state of
the TTL input.

The actual DC voltage level is controlled by the
contrast control circuitry. The programmed contrast
DC level is provided by circuitry on the I/O board.
Refer to Chapter 6 for details of this signal.
Potentiometer R5 provides manual adjustment of the
level actually presented to the emitter-follower
amplifier formed by transistor Q1. Resistor R6 and
capacitor C4 make up a low-pass filter that provides
smoothing of the incoming DC contrast level.

Transistor Q1 is connected as an emitter-follower in
order to provide the high current required to drive
the low impedance of R8. The higher the voltage on
R8, the larger the contrast between black and white
in the final pixel on the CRT.

Note that there are no gray levels in the Lisa video
circuitry. Gray tones can be generated by pixel
interleaving under software control. The details of
this lie outside the scope of this manual.

7.3.2 Cathode Drive Circuit

The collector output of transistor Q6 is passed on
to the base of the stacked transistor pair Q2/Q3.
The advantage of this circuit is that it combines
the advantages of the high gain of Q3 with the
ability to withstand high voltages of Q2. Capacitor
C6 and resistor R11 are used for high-frequency
peaking. Resistor R1Ø prevents transistor Q2 from
going into cutoff when the screen is blank.

The collector load for Q2 consists of the peaking
coil L1 and collector load resistor R14, with R13
providing a shunt to damp L1. The collector voltage
on Q2 is dependent on the polarity of the pixel
being displayed. For black, it is about +6Ø VDC,
while for white it is from 1Ø to 3Ø V lower. The

exact voltage level for white depends on the setting
of the contrast R5 and the input DC contrast level
at pin B on the board control circuit.

The flyback transformer assembly at B-2 of the
schematic provides a +6∅ VDC power source at pin 2
on connector P-3. This is filtered by the storage
capacitor C8. Capacitor C7 and diode CR3 form a
decoupling network, which ensures that the beam
current to the cathode is removed when the Lisa is
turned off. This is known as a "spot-killer" and
prevents phosphor burn at one point on the screen.

The output of Q2 is passed through the 22∅ ohm
arc-protecting resistor in the cathode lead. This
prevents any arcing voltages in the tube from
reaching the video amplifier circuitry. Diode CR2
is normally reverse-biased. In the case of an arc
occurring in the CRT, this shunts the high-voltage
on the lead, acting as an arc-suppressor. The lead
connects to pin 2, cathode, of the CRT itself.

7.4   Vertical Deflection Circuit

The vertical deflection circuit positions the horizontal
scan of the CRT at the appropriate position in the
vertical axis. It is shown in the left center part of
the schematic, and consists largely of integrated
circuit U2 and its associated components.

Vertical synchronization pulses are provided by the
processor board on pin A of the connector. This TTL
signal is passed through coupling capacitor C9 and
current-limiting resistor R17. The resulting signal
pulses are fed into the input of the TDA 117∅ at pin 8.

7.4.1 Vertical Deflection Oscillator

The resistor/capacitor (RC) network formed by C1∅
and R19/R2∅ provides a timing period for the
oscillator internal to U2. Potentiometer R19
enables the period to be varied into synchronization
with the periodic screen refresh. This acts as a
vertical hold. The network connects to pins 6 and 9
of U2.

7.4.2 Vertical Voltage Amplifier

Internal to U2 is a circuit used to control the
amplitude of the vertical deflection.

The gain of this amplifier is controlled by the
amount of current sunk to ground from pin 7 of U2.
This is a function of the resistance provided by R21
and R22. Potentiometer R22 allows this value to be
varied; this adjusts the amplitude of the vertical
saw-tooth voltage and thus the physical height of
the display on the CRT.

The voltage amplifier output is present on pin 1 of
U2. It is utilized in two distinct places:

> 1. As an input to the feedback network
>   formed by R31, R32, C15, and C16. This
>   controls the linearity of the sawtooth
>   waveform that is output at pin 1. This
>   can be adjusted by potentiometer R31.
>   The network feeds back to pin 12 of U2.
>
> 2. As an input to the power amplifier stage
>   through summing resistor R29 to pin 10 of
>   U2.

7.4.3 Vertical Power Amplifier

Input to the power amplifier is at pin 10. The
amplified output is available at pin 4 of U2. The
output signal follows four paths:

> 1. It is fed back into the power amplifier
>   via C14 and R27 to limit the
>   high-frequency response and to prevent
>   parasitic oscillations.
>
> 2. It is passed through the vertical
>   deflection coils via pins 1 and 2 of
>   connector P1 and is passed to ground via
>   resistor R33 and capacitor C19.
>
> 3. It passes through the snubbing network
>   R25 and R17 to ground. The circuit is in
>   shunt with the deflector coils and
>   prevents any ringing effects in the coils
>   themselves.
>
> 4. It takes the signal DC component, sampled
>   by R26 and filtered by C18, and passes it
>   on to the summing resistor R28, and so to
>   the amplifier input signal on pin 10.
>   This signal is used to establish the DC
>   operating point of the power amplifier to
>   ensure DC stability.

AC current passing through the deflection coils is

sampled across R33, fed through summing resistor
R3Ø, and also presented as a component of the input
signal on pin 1Ø. This controls the AC voltage gain
of the power amplifier and enhances AC stability.

7.4.4 Bootstrap Circuit

The power input to U2 is pin 2, which should have a
DC voltage between +11 and +16 VDC. This is
provided by the voltage drop from +28 V, which in
turn is provided by R24 with storage capacitor C12.
This voltage is also used to provide the collector
supply for the emitter-follower circuit of Q1 in the
video-amplifier section.

Part of the output signal of the power amplifier,
presented at pin 4 of U2, is also presented at pin
5. This forces pin 5 above the DC input voltage at
pin 2 and reverse-biases CR5.

This forces pin 3 above the DC input voltage because
of the charge stored in C11.

7.5 Horizontal Deflection Circuits

The horizontal deflection circuits provide the timing
and control of the sweep of the beam across the CRT in
the horizontal direction.

The horizontal frequency of the Lisa video circuit is
approximately 22.7 KHz.

7.5.1 Horizontal Input Circuit

The horizontal drive pulse is a TTL signal provided
by the processor board and presented to the video
board on pin C of the connector.

Summing resistor R53 presents the signal to Q7,
which operates as an adjusted Miller integrator.
Adjustment is achieved by controlling the amount of
feedback to the input by way of the horizontal
phase-control potentiometer R34. Feedback to the
base of Q7 is by way of resistor R36 and the Miller
capacitor C2Ø.

This circuit controls the amount of rise and fall
time in the output signal by means of the Miller
effect. This controls the switching point of Q8 in
time, which operates as a high-speed saturated
switch.

7.5.2 Horizontal Sweep Amplifier

The output of Q8 is used to drive the base of the
horizontal driver transistor Q4. The output of Q4
is in turn coupled to the base of the horizontal
output transistor Q5 by way of the coupling
transformer T1 and the base-current limiting
resistor R45.

The RC network formed by R41 and C24 is used to
control the damping across the primary windings of
T1. Similarly, R44 is used to damp the secondary
windings.

Power for the driver stage of the amplifier is
derived from the +28 VDC supply via the decoupling
network formed by R39 and C23.

7.5.3 Horizontal Deflection

Transistor Q5 turns off when the base voltage goes
negative. When this occurs, the stored current in
the horizontal flyback transformer and the
horizontal deflection coils collapses. This causes
the collector voltage of Q5 to rise to approximately
280 V. The rate of rise is controlled by the timing
capacitor C25, which lies between the collector of
Q5 and ground. Diode CR9 is used as a damper to
prevent the collector of Q5 from going negative by
passing the negative half of the current cycle to
ground.

Energy is coupled out of the horizontal circuit by
way of the flat-faced correction capacitor C26.
Current is then passed through the horizontal
deflection coils, through the horizontal linearity
coil L2, and to ground. Coarse picture width is
controlled by varying the inductance of L3, which is
in parallel with the deflection coils.

Coil L2 increases the linear current ramp through
the deflection coils. A magnet in the coil is used
to bias the coil-1 in one direction. As current is
passed, this adds to or subtracts from the magnetic
bias. This in turn alters the value of the
inductor. R46 is used to damp any high-frequency
oscillation within the horizontal deflection coil
circuit.

7.5.4 Horizontal Flyback

The flyback transformer also connects to the
horizontal output transistor Q5. It is used to step
the voltage on the collector of Q5 either up or
down.

This is used to generate the high-voltage supply for
the CRT at 13K VDC, the 6Ø VDC supply for the video
amplifier and also +6ØØ VDC for the G2 voltage on
pin 6 in the CRT. It also provides power for the
brightness and focus circuit, which is physically
located on the power supply board in order that the
controls are available to the operator of the Lisa.

Power input to the flyback assembly comes from the
+28 VDC supply on pin 3, violet.

A portion of the horizontal output signal is coupled
by C27 to R47 and CR1Ø. This provides a -1ØØ VDC
source to operate the brightness and focus
circuits.

7.5.5 Overvoltage Crowbar

The voltage at the collector of Q5 is sampled by the
precision divider formed by R42 and R43. This is
fed through the peak-detector circuit formed by CR8
and C22 and placed on the cathode of CR7. If the
voltage on the collector of Q5 should rise above
acceptable limits, CR7 conducts and provides a
forward bias on SCR CR6. This latches CR6 on,
shunting the collector supply of Q8 to ground. It
also turns the horizontal circuits off and avoids a
damaging high voltage on Q5. SCR CR6 remains in
this condition until power is removed from the
Lisa. It also prevents excessive voltage to the
CRT, thus keeping it within the safe X-ray rating of
the tube.

7.5.6 Brightness and Focus

The control circuits for these two functions are
logically a part of the horizontal deflection
circuit, but are physically a part of the Lisa power
supply for ease of operator access to these
controls.

The +6ØØ VDC high-voltage power for these circuits
is provided by the components CR11, R48, and C33
from the secondary windings of the flyback
transformer. The negative voltage comes from

components C27, R47, and CR1Ø.

The brightness of the CRT is controlled by
adjustment of the DC voltage on pin 1, the control
grid, of the CRT. This can vary from +12 to -38 VDC
with respect to ground, and is adjusted by means of
the 2 V megohm resistor marked Brightness.

The focus is a voltage placed on pin 7 of the CRT.
It can vary between -1ØØ and +3ØØ VDC, depending on
the adjustment of the 2 megohm resistor marked
Focus.

CHAPTER 8. USER INTERFACES
_____

The Lisa uses the CRT and a speaker to communicate with the
user. The user can communicate with the Lisa by using the
mouse and keyboard. In addition, there is a video jack
available on the motherboard at the back of the Lisa that
supplies a composite video signal and can be used to drive a
secondary CRT.

8.1   The CRT

The CRT is controlled by a combination of Lisa software
and hardware elements on both the processor and video
boards. Refer to section 4.5 and to Chapter 7 for a
discussion of the hardware.

8.2   The Keyboard

The 76-key Lisa keyboard is a detachable assembly that
contains a full key-set and function keys. It is
connected to the Lisa by a standard 1/4 inch stereo
phone jack, located above the on-off button on the front
of the cabinet. The standard keyboard layout, North
American, is shown in Figure 8-1. Appendix H contains
all available Lisa keyboard layouts.

8.2.1 Keyboard Logic

The keyboard logic is shown in schematic Ø5Ø-4ØØ1 in
Appendix E. It operates under control of the COPS
device shown on the schematic at C-1.

The COPS is identical to that found in the keyboard
control logic on the I/O board. Refer to section
6.5 for details of this. The same routines are
present in both devices. Only the routines that
apply to the location of the device are used.

Figure 8-1. Standard Keyboard Layout

The keys interface to five 4Ø67 16-to-1 multiplexer
devices. The COPS polls these in an upper and lower
bank by means of the SK signal and the LSØ3 gate at
C-2. The configuration of the COPS DØ-D3 outputs
defines which of the sixteen switches attached to
each device is being selected.

US NEW Keyboard Layout

TN / 8 ... V, 82

LEGEND

◄] Left
[► Right
[▲] Up
[▼] Down

▦ Dead key, no character is generated until next key is pressed.

↷ Character has lower case and is affected by Caps Lock.

OPTION Selects Alternate Keyboard

Left; | Right;
Primary keyboard | Alternate keyboard

```
┌─────────┐
│ P    Π  │   Upper: Shifted
│ ↷    π  │   Lower: Unshifted
└─────────┘
```

Boldface indicates that the character is printed on the keytop.

When no character is shown in the lower area of the keytop, one of the following is true:

a. If the symbol ↷ is shown, the lower character is the lower case equivalent of the upper character.

b. If the symbol ↷ is not shown, the lower character is the same as the upper character.

The state of the switches in the bank of 4Ø67
devices is presented to the COPS on the three lines
G1-G3. The lower bank uses all three but the upper
bank uses only G2 and G3.

Key data are passed to the Lisa in serial form from
the SØ output of the COPS via the LSØ3 gates at B-1
and pin 1 of the Molex connector. Synchronization
pulses from the Lisa are also input to the keyboard
on pin 1 and passed to the GØ input of the COPS via
the final LSØ3 gate at B-1.

8.2.2 Keyboard Timing

Transfer of data from the keyboard to the Lisa is
performed when the keyboard controller initiates
it. This is shown in Figure 6-13. The keycodes are
discussed in section 2.4.5.

Data transfer is initiated when the keyboard-data
line is pulled low by the Lisa for approximately 2Ø
microseconds. The keyboard COPS senses the leading
and trailing edges of this SYNC pulse and transmits
an ACK pulse to indicate to the keyboard controller
that data are about to be transferred.

A data byte that specifies the key is transferred in
a lower and upper nibble as shown in Figure 8-2.
The byte is interpreted as a key and a polarity, up
or down, by the keyboard controller.

If no data are present in the keyboard COPS, no ACK
pulse is sent. The interface becomes quiescent
until the next SYNC pulse.

8.2.3 Keyboard Interface

The keyboard interface to the Lisa consists of a
3-wire shielded cable which is terminated by a 3-pin
Molex connector attached to the keyboard PCB at one
end and a standard 1/4 inch stereo phone jack plug
at the other. This arrangement is shown in Figure
8-2.

Figure 8-2. Keyboard Interface

8.3   The Mouse

The mouse is an electromechanical device that provides
communication with the Lisa software in addition to the
keyboard. It consists of a rolling ball arrangement on
the under side and a plastic cover with a button on the
top. A cable connects the mouse with the 9-pin DB
connector in the center of the motherboard at the back
of the Lisa.

The specific functions of the mouse depend on the
software currently running. However, the two controls
on the mouse provide the same general function in all
cases:

        * Rolling the mouse around a flat surface
          moves a cursor around the screen, and

        * Pressing the button on top of the mouse
          selects the item or software function at
          the cursor location.

8.3.1 Internal Components

        The internal components of the mouse consist
        basically of a switch and two directional wheels.
        One directional wheel detects motion forward and

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+5v ←

Host Connection Signal ←

Red (+5v)

Black (digital ground)

Shield to chassis ground

White (signal)

Shield to Keyboard Chassis

Keyboard Connection

White (1)
Black (2)
Red (3)

to +5v
to digital ground

to Signal

Figure 8-2. Keyboard Interface

8-4b
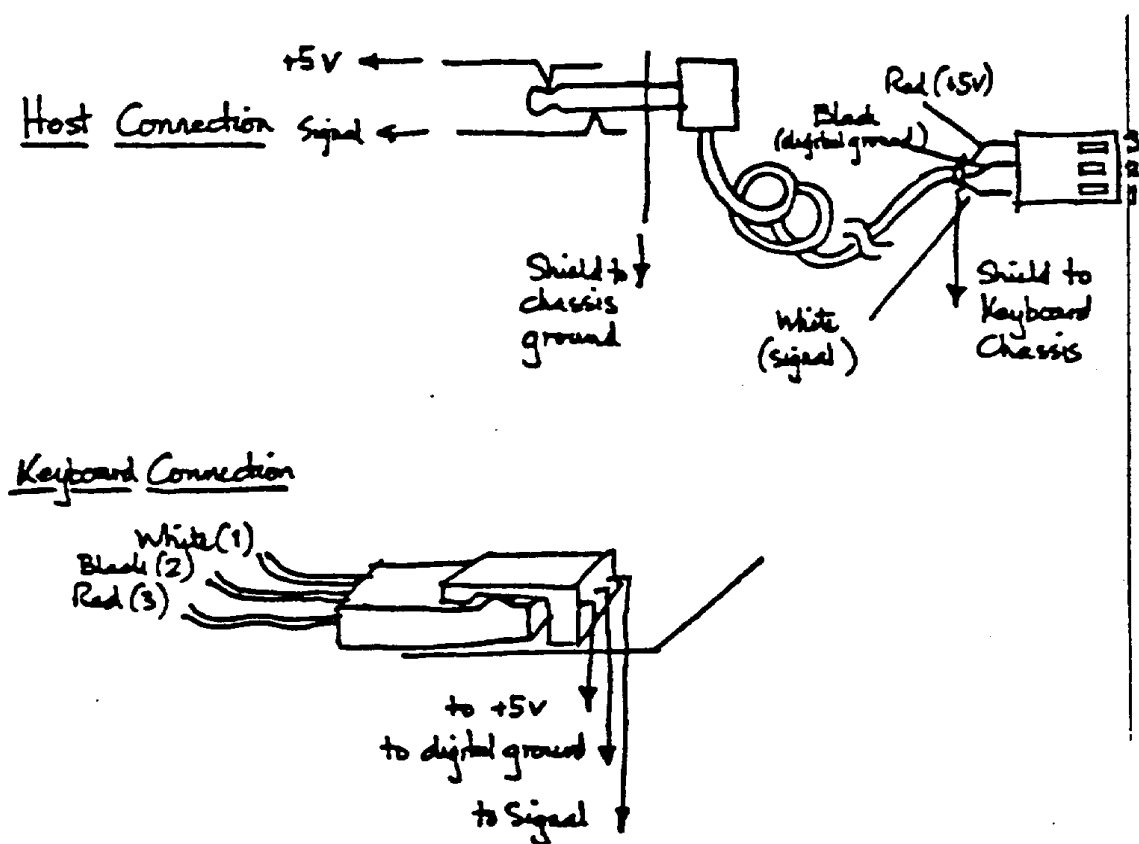
back, corresponding to up and down on the screen,
while the other detects motion left and right.

Each wheel has a number of slots cut around the
rim. These pass two photoelectric diode assemblies
as the mouse is moved in that axis and the wheel
turns. The two diode assemblies produce a series of
pulses to the mouse interface on the I/0 board.

The relationship of one set of pulses to the other
indicates the polarity of the direction in which the
mouse is moving, and the number of pulses is
proportional to the distance travelled. Refer to
Figure 8-3, which illustrates this.

8.3.2 The Mouse Interface

The mouse interface is briefly described in section
3.5. The 9-pin DB connector is located in the
middle of the connector panel at the back of the
Lisa. Refer to Figure 3-11 for the connector
layout.

Only SWITCH0 is operational in the mouse. Each pair
of the LEFT/RIGHT and UP/DOWN inputs pulses, as
shown in Figure 8-3, when the mouse moves one
increment in that direction. One increment equals a
constant unit of movement in that direction on the
flat surface.

Figure 8-3. Mouse Movement Waveforms

Figure 8-3. Mouse Movement Waveforms

8-5b
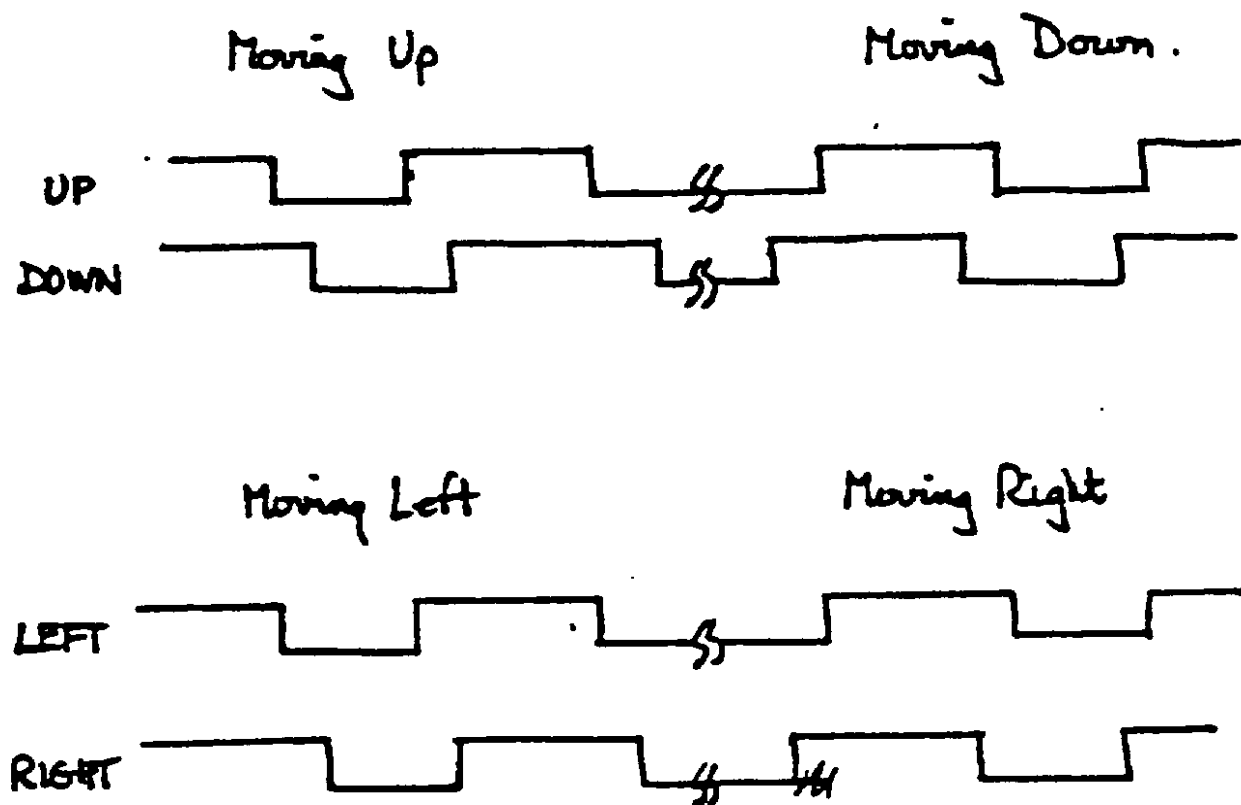
8.4   Other User Controls

Several user-oriented features of the Lisa are described
elsewhere in this manual in more detail but are
mentioned here for convenience.

8.4.1 The On-Off Switch

The on-off switch is located on the front of the
cabinet, in the lower-right corner. Pressing this
switch when the Lisa is off sends power to all parts
of the Lisa under control of the boot software.

Pressing this switch when the Lisa is on causes an
interrupt to software which in turn cleans up its
environments and then ejects any floppy disks in
use. The Lisa is then turned off under software
control. This turns off everything except the
control COPS, which handles the RTC and power-on
control. The control COPS receives its power from a
standby supply in the power supply. Refer to
section 1∅.5 for details.

Whenever the Lisa is isolated from a power source,
perhaps because the Lisa is disconnected or the
power fails, a self-recharging battery maintains the
voltages necessary to operate the standby supply
voltages for a period up to approximately 1∅ hours.
The battery is automatically recharged whenever the
Lisa is turned on. Refer to section 6.7 for a
discussion of this.

8.4.2 The RESET Switch

The RESET switch is located on the motherboard at
the back of the Lisa, next to the video connector.
RESET is used to restart the Lisa in the event that
an unrecoverable error has put the Lisa in an
undefined state. This should never be activated
during normal processing or loss of data almost
certainly results. The reset switch is shown at
location C-2 on the motherboard logic schematic
∅5∅-4∅13 in Appendix G.

8.4.3 The Speaker

The built-in speaker can be used to provide an
audible warning to the user. It is controlled by
logic on the I/O board under software control for

volume and tone. Refer to section 6.7 for a
discussion of speaker control.

8.4.4 The Composite Video Output

The composite video output is available on the J1Ø
video jack at the back of the motherboard. The
circuit is located on the motherboard and uses the
CVOUT and VID signal outputs from the processor
board. Refer to section 4.5. The composite video
signal is output to the jack via resistor R2.

The logic is shown on schematic Ø5Ø-4Ø13 in area
C-2. Both the VID and CVOUT signals are effectively
ORed to the base of transistor Q2. This controls
the amount of current passing through Q2 and
consequently through R7, which controls the amount
of current passing through Q1.

CHAPTER 9. FLOPPY-DISK DRIVES

_____

The Lisa is equipped with two floppy-disk drives for data file storage. These are located one above the other at the right side of the cabinet. They interface to the Lisa by means of a floppy-disk controller, which is located on the I/O board and is described in section 6.2.

This chapter does not present an exhaustive description of the drive. Refer to other documentation on the disk drive for further details.

9.1   Specifications

Capsule summaries of disk-drive specifications follow.

9.1.1 Media

Disk size . . . . 5 1/4 inch
Media . . . . qualified double-sided
                                10,000 FCPI
Track density . . . . 62.5 TPI

9.1.2 Speed

Motor speed settle time . . . . . . 150 msec
Motor on time . . . . 400 msec
Head settling time . . . . 10 msec
Carriage movement . . linear stepper actuator
Spindle rotation . . . . DC Motor

9.1.3 Electrical

+5 VDC standby. . . . . 75 mA
+5 VDC running . . . . 80 mA

+12 VDC standby . . . . 42 mA
+12 VDC running . . . . 850 mA
+12 VDC maximum (during motor start) . . 1.6 A
-5 VDC standby . . . . 5 mA
-5 VDC running . . . . 8 mA

9.1.4 Environmental

See section 3.2, Lisa Specifications.

9.2   Drive Block Diagram

The floppy-disk drive is an assembly that enables 5-1/4
inch flexible diskettes to be used as data storage
media. In the Lisa, there are two functionally
identical drives controlled by logic on the I/O board.

The drive itself can be thought of as consisting of a
number of component blocks, as shown in Figure 9-1. The
motors and detectors present in the drive chassis are
directly controlled by the digital board, while the head
read/write functions are performed by the analog board
under control of the digital board.

Figure 9-1. Drive Block Diagram

9.3   Drive Interface

The interface to the drives is performed in the Lisa by
signals provided on motherboard connector J1, under
control of the I/O board's floppy-disk controller.
Refer to section 6.2.
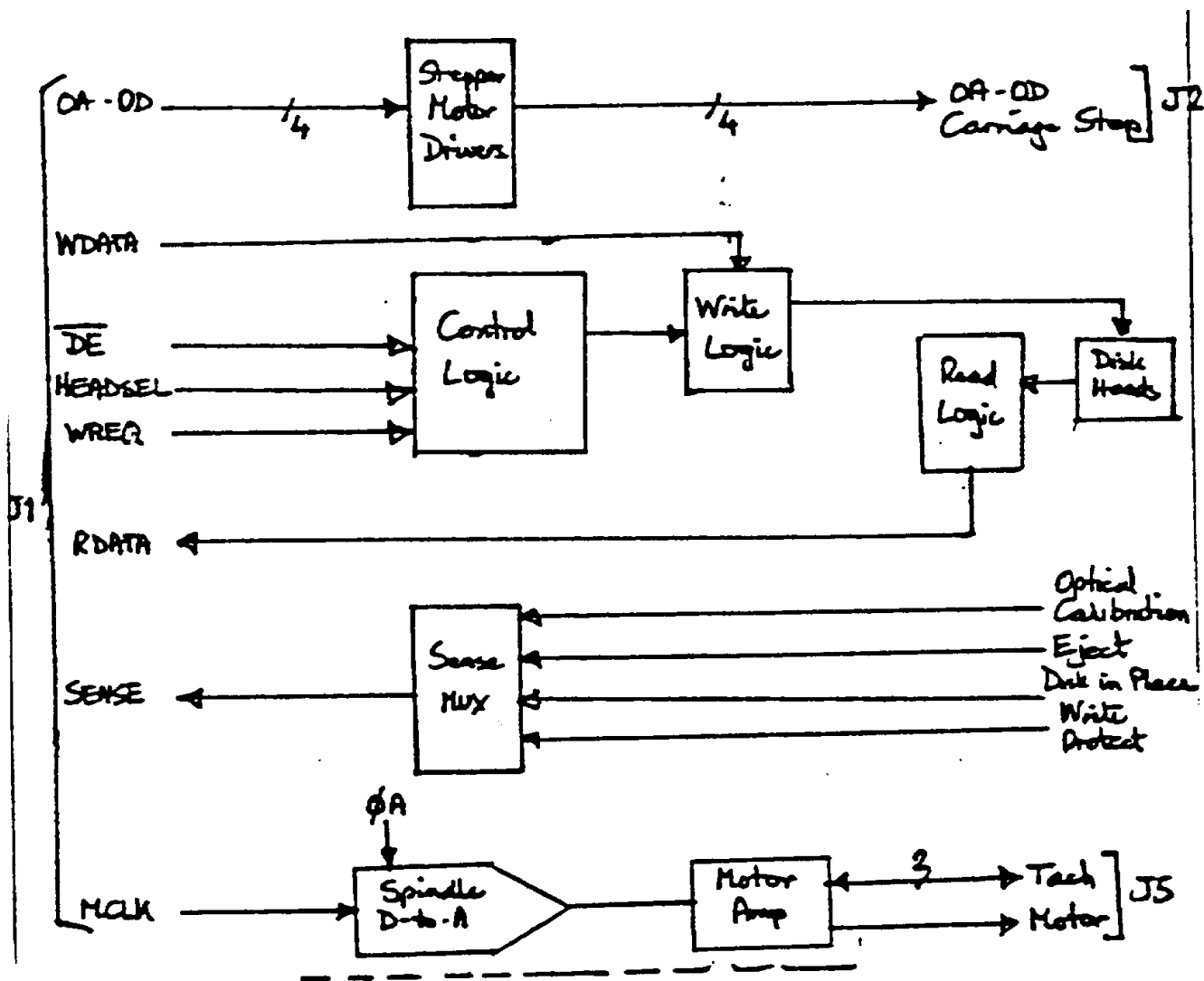
Figure 9-1. Drive Block Diagram

9-2b

9.3.1 Drive-Interface Signals

The interface signals to the drive are shown in
Figure 9-2.

```
Signal        Pin #         Signal

             |    |     |
+12 VDC      | 1  | 2   | Phase Ø/motor data/sense select
+12 VDC      | 3  | 4   | Phase 1
+12 VDC      | 5  | 6   | Phase 2
+12 VDC      | 7  | 8   | Phase 3
 Ground      | 9  | 1Ø  | Write Data
 Ground      | 11 | 12  | /Write Request
 Ground      | 13 | 14  | Read Data
 Ground      | 15 | 16  | /Drive Select
not used     | 17 | 18  | Head Select
not used     | 19 | 2Ø  | Sense
+5 VDC       | 21 | 22  | Motor Data Clock
+5 VDC       | 23 | 24  | /IRQ
+5 VDC       | 25 | 26  | not used
             |____|_____|
```

Figure 9-2. Drive-Interface Signals

9.3.2 Drive-Interface Timing

The density of data written on the disk is a
function of the floppy-disk controller and the
capacity of the medium to store bit transitions.
Refer to sections 6.2 and 6.3 for a discussion of
controller operation.

Timing of the stepper motor that controls head
movement is defined by the four phase lines on the
interface. These are manipulated to move the heads
forward or backwards.

In order to avoid inaccurate head positioning due to
mechanical tolerances in the carriage mechanism, all
seeks finish with a final motion in a direction
towards the optical calibration point. Note that
this means that the upper head is moving away from
the spindle while the lower is moving towards it.
Refer to Figure 6-11.

In order to overcome the inertia during carriage

acceleration and deceleration, three different
periods are employed between speed transitions on
the phi lines. This can be seen in Figure 9-3.

Figure 9-3. Carriage Movement Timing

In the quiescent state, all four phase lines are
low. Motion is begun by asserting two of the
lines. In the forward direction, towards the
optical calibration point, this would mean phi3 and
phi∅; in the reverse direction, phi∅ and phil. At
the end of the first period, one phase is deasserted
and another asserted, as shown in Figure 9-3. Note
that one phase remains on while others are being
changed.

When the carriage is at the required position, phi∅
is always the last phase to remain asserted alone
for the final period before all phases are again
deasserted and the carriage is at rest.

Figure 9-3.   Carriage Movement Timing

9-4b
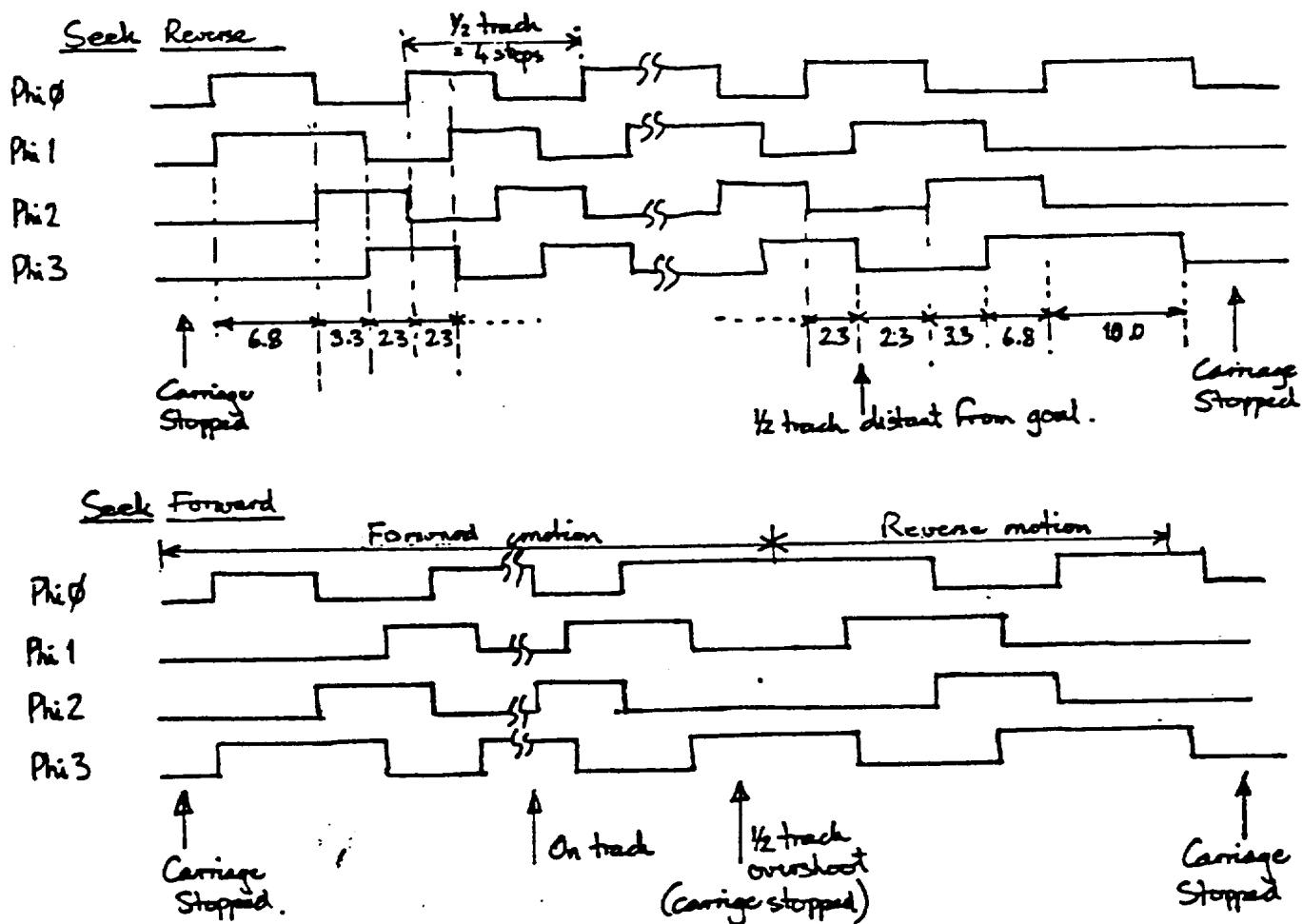
Note that for a seek in the reverse direction, the
carriage is brought to a halt four steps beyond the
desired position, and then a seek forward of four
steps is made to restore the head to the
center-track position. This operation is known as
overshoot.

Each step corresponds to 1/8th of a track. Thus all
tracks are eight steps apart. In the case of
difficulty in reading data from the required track,
the floppy-disk controller attempts to offset by
1/8th track steps to allow for misalignment.

The optical disk calibration signal is available to
the controller as an aid in overcoming differences
in mechanical alignment between disks. It provides
an accurate radial reference point from which seeks
can be made. This is also known as the recalibrate
function.

9.4   Basic Drive Operation

The drive is capable of performing a number of
operations under control of the signals on the drive
interface. The operations are described in following
subsections.

9.4.1   Inserting and Removing Disks

When a floppy disk is inserted in the drive, the
eject mechanism is armed and a switch is activated
to indicate that the disk is in place. This can be
detected by the controller on the STATUS signal
line, pin 2Ø, if both the HEADSEL, pin 18, and the
phiØ, pin 2, are asserted by the controller.

Pressing the eject button on the front of the drive
causes a line to be asserted in the drive. This
state can be detected on the STATUS line by holding
the HEADSEL signal asserted with the phiØ signal
deasserted.

The controller should then move the heads away from
the disk until the disk-in-place signal becomes
deasserted. At this point, the heads should be
moved nine tracks further in order to activate and
reset the eject mechanism.

9.4.2 Loading Disk Heads

When a disk is detected in the drive, the disk heads
can be loaded. This is performed in the sequence
below. Namely, the:

* Drive motor is activated and brought up to
  speed,

* Centering cone is pressed into the disk
  hole,

* Spindle begins rotating,

* Disk is clamped to the spindle,

* Heads are moved inward towards track 45,

* Head load mechanism presses the heads
  against the disk surfaces.

The steps in the above sequence are performed
mechanically when the carriage is being moved to
bring the heads over the disk surface. The spindle
begins to rotate when clock pulses are presented to
the spindle motor control via the MCLK line on pin
22.

The spindle is already spinning before being brought
into contact with the disk. The clamper forces the
disk to be seated centrally on the spindle with the
rotation of the spindle assisting in this.

The heads are moved by pulsing, in the correct
sequence, the four control lines of the stepper
motor:

* phi0, pin 2
* phi1, pin 4
* phi2, pin 6
* phi3, pin 8.

9.4.3 Positioning Heads

The two read/write heads in the drive are mounted on
a single carriage that is driven by a head
positioning actuator. This consists of a linear
stepper motor and lead screw.

This mechanism not only provides head-to-track
positioning but also actuates a disk clamping and
unclamping mechanism. The mechanism clamps the disk

as the heads are moved into the reading surface and
unclamps it as the heads are moved clear of the
surface.

9.4.4 Data Read/Write

The ceramic heads in the drive operate in direct
contact with the disk surfaces. Each head is a
single element with straddle erase elements to clear
the inter-track gap.

During a read operation, the heads transform the
polarity reversals on the disk surface into a stream
of analog pulses. These are converted to serial
digital data and presented to the controller as the
RDATA signal on pin 14. It is the function of the
controller to interpret this data.

The write circuitry takes the serial digital data
presented on the WDATA line, pin 1Ø, by the
controller and converts it to the correct analog
pulses for the write heads.

Data are written to whichever head is currently
selected, depending on the write protection
condition of the disk currently in place. The
controller senses the write protection condition of
a disk by deasserting both the HEADSEL and AØ
signals before polling the SENSE line.

The write-protect sense condition informs the
controller that the disk currently inserted has its
write-protect slot uncovered. There is a hardware
protection circuit in the drive to inhibit writing
to a disk that is write-protected. It is a function
of the controller to decide whether or not the disk
will be written to. Currently, the floppy-disk
controller does not write to a protected disk.

CHAPTER 1Ø. POWER SUPPLY

The power supply is a flyback-type switcher supply. The circuit diagram is shown in schematic Ø5Ø-4Ø11, which can be found in Appendix F. The supply provides the power levels and voltages shown in Figure 1Ø-1.

Voltage	Variance	Current
+ 5 V	+/-5% (5.25 V/4.76 V)	4.ØØ to 8.ØØ A
+12 V	+/-8% (13.Ø V/11.1 V)	Ø.35 to 2.ØØ A
+33 V	+36 V Max. +32 V Min.	Ø.3Ø to Ø.7Ø A
- 5 V	+/-1Ø% (-5.5 V/-4.5 V)	Ø.ØØ to Ø.2Ø A
-12 V	+/-1Ø% (-13.2 V/11.8 V)	Ø.Ø1 to Ø.2Ø A
+5 VSTBY	+/-5% (5.25 V/4.75 V)	Ø.ØØ to Ø.1Ø A

NOTE: The standby +5 V is not switched off by the on-off signal.

Figure 1Ø-1. Supply Current Output

In addition to the main power supply, an auxiliary standby supply is required. The standby supply provides the minimal +5 V power required to run the soft-power-on and real-time clock circuitry while the Lisa is in a power-off condition.

The focus and brightness controls for the CRT are located on the power supply and are accessible from the back of the Lisa. They are placed here for the user's convenience; there are no internal electrical connections between these controls and the power supply proper. All power output lines are fully isolated from the input AC power by means of transformers or opto-isolators.

10.1   Power Supply Block Diagram

The Lisa power supply consists of the following major
components shown in Figure 10-2:

* AC input circuitry
* Flyback oscillator
* DC output circuitry
* Standby power supply
* Video focus/brightness
* Front panel control
* Safety interlock
* Over-temperature monitor.

As can be seen from Figure 10-2, both conducted and
radiated noise generated by the switcher are reduced by
the input filter on the AC line. The input AC power is
then rectified and filtered before being presented to
the main flyback oscillator.

The flyback oscillator operates by storing a controlled
amount of energy, in the form of a magnetic field, in
the switcher-transformer core during the forward cycle
as the core is being charged. During the flyback cycle,
the core discharges this energy to the load placed
across the secondary windings.

The secondary windings are connected to the secondary
rectifier and filter circuits which provide the DC power
outputs. These outputs are monitored by a regulator
circuit, which senses the voltage level and adjusts the
power being provided. In addition, there is a crowbar
circuit that shuts the power supply down if the output
voltages exceed the preset limits.

Figure 1Ø-2. Power Supply Block Diagram

1Ø.2 AC Input Circuits

Refer to schematic Ø5Ø-4Ø11 in Appendix F. The AC input
circuits are shown in the upper left quadrant.
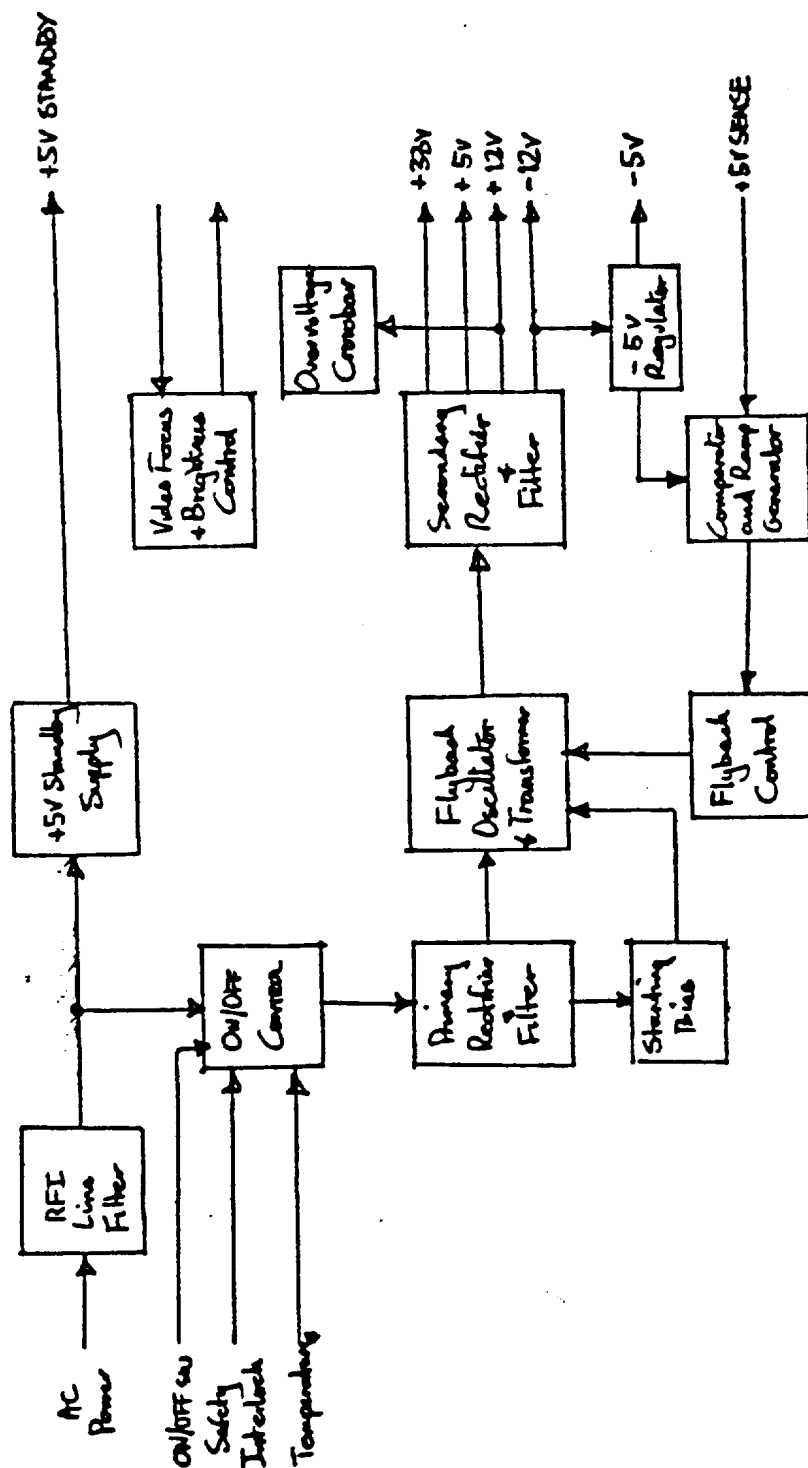
Figure 10-2. Power Supply Block Diagram

10-3b

10.2.1 AC Line Connection

The AC connector P3 supplies power via the power
cord and inductor L7 to the J2/P2 connector. This
presents the power to the input line filter, which
consists of transformer T1, chokes L1 and L2, and
capacitors C1, C2, C3 and C4. Thermistor R9 and
fusable resistor R8 are provided to limit the inrush
current to the power supply.

10.2.2 On-Off Control

Power to the supply is controlled by opto-isolator
U3, which controls the switching triac CR2. U3 is
provided with +5 V from the standby supply via Q5,
which biases a light-emitting diode between pins 1
and 16. Pins 8 and 10 operate as a photosensitive
Triac. Power is switched to the main supply via
CR2.

Resistor R33 is a temperature-sensitive varistor,
which biases Q6. Excessive temperature causes Q6 to
draw enough current to ground out pin X and to turn
off the supply.

The power supply is switched on by applying a logic
1 level to the base of transistor Q5, causing
transistor Q5 to conduct, which grounds pin 1 of
U3. The power supply switches on and stays on until
this level is removed.

A low level on the base of Q5 keeps the power supply
in the OFF condition. This can be achieved by
either driving it low via the software on-off or by
grounding the safety interlock switch.

Warning: Note that the power supply itself remains
powered at all times when the Lisa is connected to
an AC power source. Test before touching.

10.2.3 Primary Rectification

The jumper below R9 is used to select the input AC
voltage that is being provided. If 110 V is
selected, the connection is made to the midpoint of
C12 and C13. Using these capacitors and the diodes
CR5 and CR6, the input voltage is doubled using
half-wave rectification. The DC voltage output from
this rectification and filtering is used to charge
up the core of transformer T3 through the 84-turn
primary winding between pins 23 and 24.

In the case of a 22Ø VAC line input, this voltage is
full- wave rectified, using diodes CR3, CR4, CR5,
and CR6. The resulting rectified DC voltage is
again smoothed by the filtering capacitors C12 and
C13.

Residual voltage that might be stored in the
filtering capacitors when the supply is shut OFF is
bled to ground via the large resistance provided by
R14 and R15 in series.

1Ø.3 The Flyback Oscillator

The focus of the flyback switching oscillator is
transistor Q1 and its associated circuitry in the lower
left of the schematic. A simplified diagram of the
flyback oscillator circuit is shown in Figure 1Ø-3. The
points labelled in Figure 1Ø-3 refer to the locations
where the waveforms given in the following figures can
be observed.

Figure 1Ø-3. Flyback Oscillator Circuit

Figure 10-3. Flyback Oscillator Circuit

10-5b

10.3.1 Flyback Starting Bias

In order for the oscillator to begin to oscillate
when power is first applied, the emitter of Q1 must
be biased negative with respect to its base. This
is done by isolation of the base from the emitter by
means of diode CR15.

Approximately 1 milliamp of current flows from the
emitter to ground via resistors R20 and R21. This
is sufficient to forward bias Q1 enough for it to
switch and begin the oscillation cycle.

10.3.2 Flyback Oscillator Operation

Pulse transformer T4 receives a pulse of current
each time the regulator circuit saturates. This
provides a voltage to the programmable unijunction
CR17. When the voltage at pin 2 exceeds that at pin
3, the unijunction operates as an SCR and shorts the
input.

This grounds the base of Q1, causing it to switch
off. To prevent the transistor from immediately
switching on again, C30 holds the emitter positive
for a short period of time, assuring a negative
base-to-emitter bias.

Since current no longer flows in the collector and
the primary windings of T3, the core begins to
discharge its energy into the secondary windings
that provide the output DC power.

During this time, transistor Q1's emitter continues
to be held positive by the charge in C31, which is
discharging through R40/R41 and CR15 to ground via
the primary winding 28/22.

Once this charge has leaked away, the current on C25
biases the emitter negative again to provide a
starting bias, as explained in Subsection 10.3.1
above, and transistor Q1 begins to conduct. This
causes current to flow through the collector and the
primary winding 23/24, which induces a magnetic
field in the transformer T3 core.

The waveforms at several critical points in the
flyback section are shown in Figure 10-4. The
letters correspond to the positions where these can
be observed.

The parasitic winding of transformer T3 provided by
the primary 25/26 is used in conjunction with CR12,

CR23, and C23 to minimize high-voltage transients,
which can be generated in T3 and could damage Q1.

Figure 10-4. Flyback Oscillator Waveforms

10.3.3 Flyback Control Circuit

The amount of power output by the supply is a
function of the amount of power that is permitted to
be stored in the core before the discharge pulse
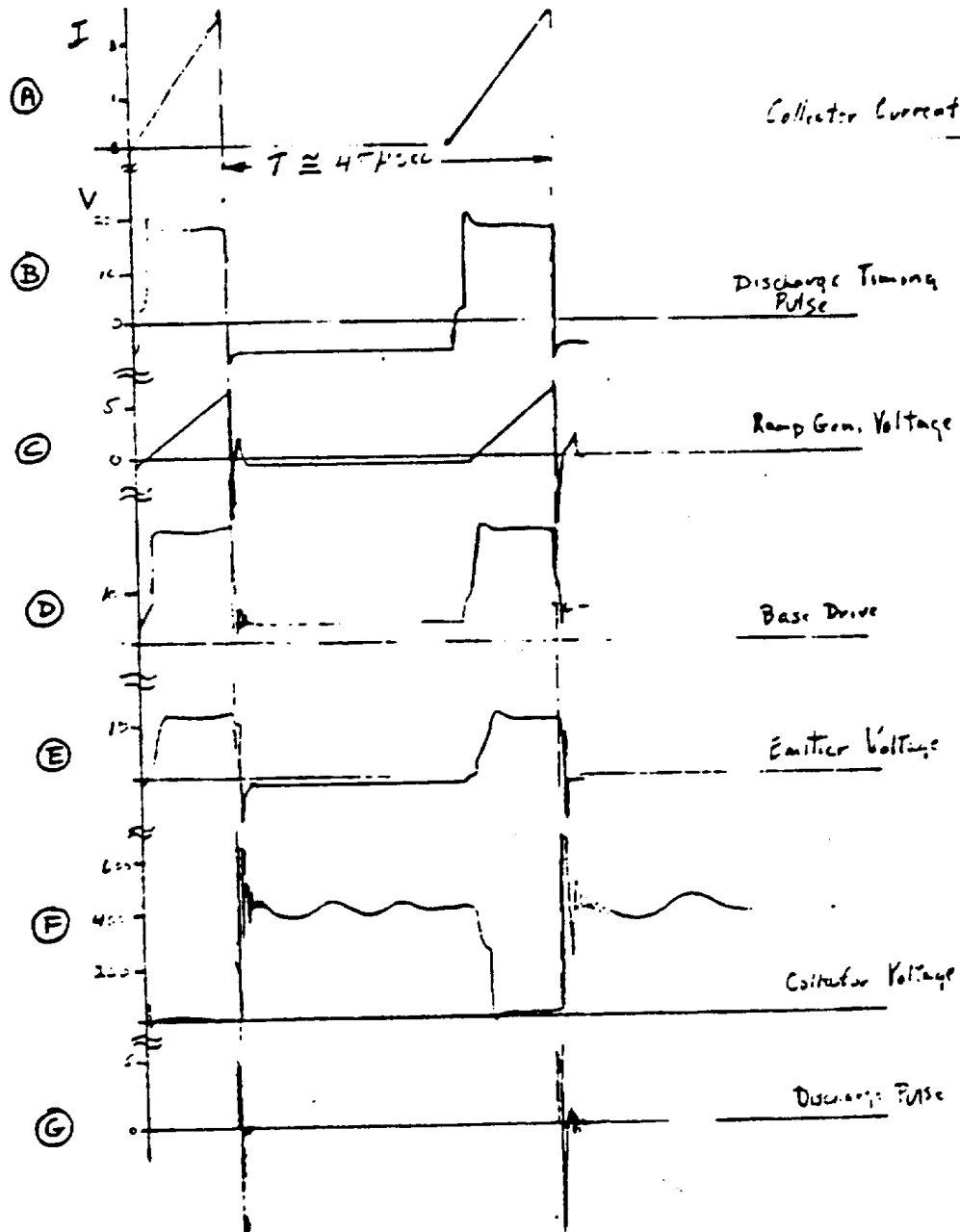
Figure 10-4. Flyback Oscillator Waveforms

10-7b

transfers it to the secondary windings. The
discharge pulse is generated by the circuits at the
lower right of the schematic. These are shown in
block diagram form in Figure 10-5.

Figure 10-5. Flyback Control Block Diagram

The level of the +5 V line is taken as the measure
of all voltage levels being presented to their
loads, since all voltages are proportional in the
switcher-type supply. This is sensed via pin N of
the terminal block and presented to the the top of
the voltage adjustment pot R29 via resistors R26 and
R27.

A -5 V reference from U2 is fed through resistor R30
and the temperature compensating diode Q4 to the
bottom of R29. When the voltages are in balance,
the adjustment tap on R29 has a nominal zero volt
bias. Otherwise, a voltage bias is applied to the
base of Q3, which operates as a voltage amplifier in
conjunction with R25 and R32.

The amplified voltage is presented to the base of Q2
through R28. This permits current to flow in
proportion to the voltage applied to its base, Q2,
operating as a voltage-controlled current source.

The path provided to the -12 V line via CR19 and R24
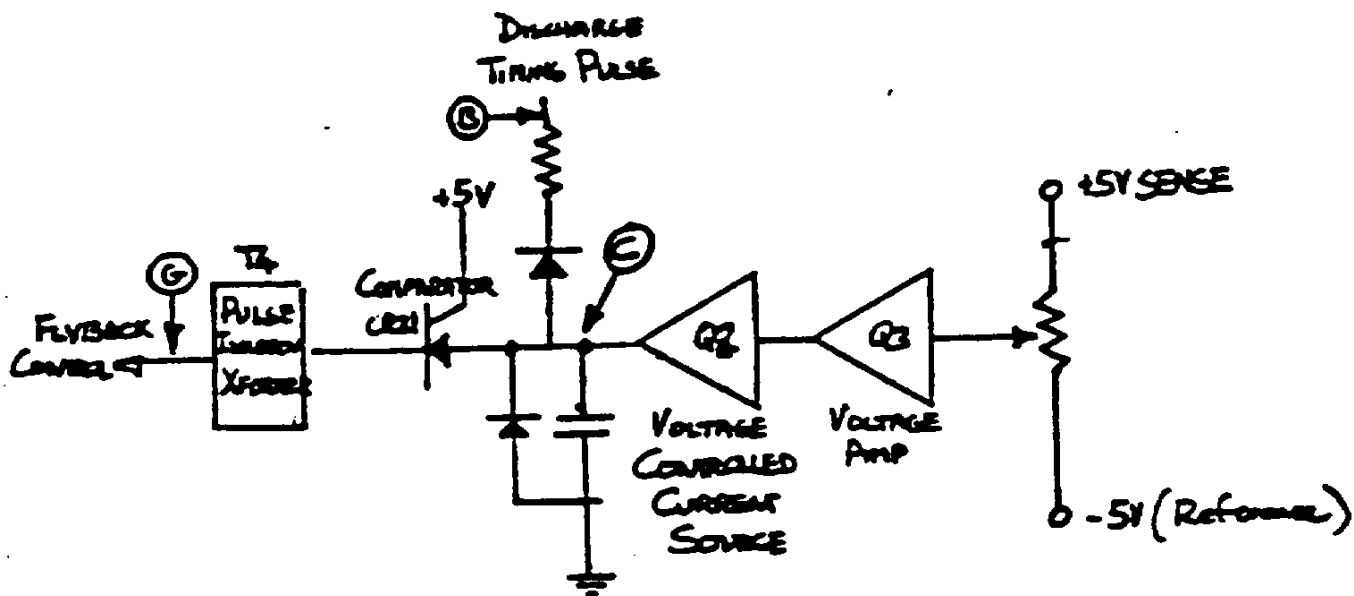
Figure 10-5. Flyback Control Block Diagram

10-8b

causes the voltage on C34 to start up from zero
volts at the same time that transistor Q1 in the
main flyback circuit is turned on. The voltage at
C34 rises at a rate in proportion to the current
being presented to it via Q2.

When the voltage reaches the +5 V level presented to
pin 2 of programmable unijunction CR21, the junction
conducts. This discharges C34 to ground, which
generates a pulse through the secondary winding of
T4. This pulse then generates a corresponding pulse
in the primary windings, which is used to turn Q1
off, as described above.

The result is a sawtooth waveform at C34. The rate
of voltage rise is controlled by the error current
from the transconductance amplifier. The total
energy stored in the switching transformer T3 is
controlled by the rate of voltage rise across C34.

10.4   DC Output Circuitry

The DC output circuitry consists of the secondary
circuits to the right of the switching transformer T3 in
the schematic. The power supply provides five voltages
from the main switcher. These are:

                    + 5 V
                    - 5 V
                    +12 V
                    -12 V
                    +33 V

Of these voltages, the last three originate in their own
separate secondary windings. The +5 V supply originates
in two windings in parallel, and the -5 V supply is
provided by a voltage regulator attached to the -12 V
supply.

10.4.1 DC Voltage Outputs

The +33 V supply comes from secondary winding 16/34
on T3, is smoothed by the C9, C10, and L3 network,
and is presented on pin D. C11 removes high
frequency noise.

The +12 V supply originates in the 20/33 winding,
with pin 20 already being biased by the +5 V supply
section. It is smoothed by C14, C15, and L4, and
presented on pins 5,9,10,E,K, and L. It is also
equipped with a crowbar over-voltage protection

circuit, described in subsection 1∅.4.2. Capacitor
C16 removes high-frequency noise on the voltage.
The +12 V supply provides the power for the
voltage-controlled current source in the oscillator
control section. Refer to section 1∅.3.3.

The +5 V supply is taken from two secondary windings
ganged together and passed through the smoothing
circuit formed by C18, C19, and C21, with C22
removing high-frequency noise. It is available on
pins 11, 12, and M.

The -12 V supply comes from the 17/34 secondary
winding of T3 and after smoothing through C27, C28,
and L6, it is placed on pin W. The -12 V supply is
also used to provide the current being fed through
Q2 in the oscillator control circuit; see section
1∅.3.3.

The -5 V supply is tapped from the -12 V supply by
means of the voltage regulator U2. It is smoothed
with C24 and presented on pin 19.

Diodes CR7, CR8, CR11, and CR18 prevent reverse
power leakage through the transformer during the
charging portion of the cycle.

1∅.4.2 DC Voltage Controls

There are two mechanisms by which the output
voltages are monitored in the power supply:

1. Voltages are maintained at the level
    selected by potentiometer R29 by means of
    the oscillator control section described
    in section 1∅.3.3. Adjustment of the pot
    raises and lowers all voltages
    proportionately.

2. Protection for the power supply load is
    provided by a crowbar circuit attached to
    the +12 V supply line. The +12 V level
    is presented to the 12 V zener CR9
    through R12. Should the voltage rise
    enough above +12 V to trigger the diode
    breakdown, the voltage is applied to pin
    3 of the SCR at CR1∅, causing it to
    conduct. This shorts the +12 V line to
    ground, which removes the current source
    for the oscillator control circuit at
    Q2. This halts the oscillation, as no
    firing of CR21 can now take place. Q1 is
    never switched off and the core ceases to

be repetitively charged, causing all
output voltages to decay to zero.

10.5   Standby and Auxiliary Video Circuits

In addition to the main switcher supply itself, two
other circuits are present in the power supply. These
are described separately because they function
independently of the main supply. The other two
circuits are the:

* +5 V standby supply and
* Video focus and brightness adjustments.

10.5.1   The Standby Supply

The standby +5 V supply is a "linear" type and is
shown across the top of the schematic. Input AC
power from the line filter is presented to the
transformer T2. The secondary windings 10/11 and
8/9 each provide approximately 10 VAC 180 degrees
out of phase. These are rectified by diodes CR1 and
CR22.

The resulting DC voltage has its ripples smoothed by
C7 and AC transients removed by C17, before being
presented to the 5 V regulator U1. The resulting +5
V output is made available on pin 20.

Note that this line has a low current capacity and
is not intended for general use.

10.5.2   The Video Controls

The video controls consist of the resistor network
shown towards the upper right of the schematic.
Focus is controlled by the potentiometer R3.
Brightness is controlled by R5.

Both potentiometers are adjusted by means of the
knobs projecting from the back of the power supply.
They receive their power from the video board via
the +300 V level on pin 1 and the -100 V level on
pin B.

CHAPTER 11. ASSEMBLIES

The Lisa is engineered to provide maximum serviceability to
the user. Refer to section 3.1 for a discussion of
packaging. A general view of the assemblies is given in
Figures 3-1 and 3-2.

Note that any nuts or screws lost in the cabinet can be
retrieved by tipping it forward. They should then slide out
of the air vents at the lower front of the cabinet. Removing
the bottom panel should not be necessary.

Section 11.1 outlines components that an user can replace.
However, the rest of this chapter is concerned principally
with components that are not user-serviceable.

11.1 User-Replaceable Components

Components that any user can replace on any functioning
Lisa include the

* Floppy-disk drive assembly
* Power supply
* Motherboard
* Processor board
* I/O board
* Memory boards
* Expansion boards
* Keyboard
* Mouse.

Access to and replacement of these components is
described in step-by-step detail in other
documentation. Refer to the Preface for a list of
related documents.

Servicing of any other components requires knowledge
about high-voltage power supplies and video
electronics. Dangerous voltages are present and all
service personnel must be trained in their use.

11.2   CRT Assembly

Refer to assembly drawing 620-5115 in Appendix I, which
shows an exploded view of the cabinet with the CRT
assembly. This assembly includes the:

* Cathode-ray tube 707-0007
* Deflection yoke 159-0007
* Video board PCB assembly 620-x121
* Video board PCB fab. 820-4012
* Flyback transformer xxx-xxxx.

11.2.1 CRT Access

Complete the following steps to remove the tube
itself. Note that you may need to refer to the Lisa
Owner's Guide to complete the first step. Handle
the tube with extreme care at all times.

! WARNING !

CRT Access can be
physically FATAL if
not performed correctly.

1. Remove the front and back panels from the
    cabinet, and then remove the power supply
    and card cage, as shown in the Lisa
    Owner's Guide.

2. Use a Phillips screwdriver to remove the
    two screws underneath the back-top of the
    Lisa.

3. Lift the top of the Lisa up from the
    back.

4. Unhook the front where it is hooked in
    place.

5. Remove the top.

6. Remove the white ground lead from the CRT
    socket. This is attached to the cabinet
    immediately above the gun.

7. Unplug the CRT socket from the end of the
    CRT. Take care not to exert too much
    pressure on the tube itself.

8. Disconnect the two yoke cables,
    yellow/green and red/blue, from the video
    board by unplugging the two 6-pin
    connectors.

9. Pry the plastic cover up from the HV lead
    that connects to the side of the CRT.

10. Press in one side of the connector under
the cover to disengage and remove the
lead.

11. The tube itself is held in place by four
screws, one at each corner. Prepare a
cushioned area on which to place the tube
upon removal. Remove the four screws
with a 1/4 inch nutdriver.

12. The tube can then be lifted out of the
cabinet with the yoke assembly still
connected.

To install the tube in the cabinet, complete the
steps above in the reverse order. Connect the CRT
socket with the CRT almost in place. Connect the HV
lead and connectors to the video board after the
tube has been screwed in place. Ensure that the
correct yoke plugs are inserted in the corresponding
sockets on the video board.

11.2.2 Deflection Yoke

Access to the deflection yoke is performed in a
manner identical to the CRT. Once the tube has been
removed from the cabinet by following the steps in
subsection 11.2.1, the deflection yoke can be slid
off the back of the CRT by loosening the clamping
screw.

Reassembly is performed in the reverse order. Once
the deflection yoke has been changed, readjustment
of picture orientation by means of the video board
controls might be necessary.

11.2.3 Video Board

Access to the video board is performed first by
removing the CRT, as outlined in subsection 11.2.1.
The procedure is then continued as follows:

1. Disconnect the cabling to the flyback
transformer from connector P3 on the
video board.

2. Release the CRT socket from the two cable
tiedowns.

3. Use a Phillips screwdriver to remove the
screws that hold the top of the video

board onto the back wall of the CRT
enclosure.

4. The board can now be removed from the
    connector on its lower edge and removed
    from the system.

To install a video board, perform the same steps in
reverse order. A new video board does not have the
correct adjustments for contrast and focus. Once
the Lisa is reassembled and operational, adjust
controls at the back of the power supply until the
picture is acceptable.

If you replace a video board, picture-size and
centering adjustment might be required. This is
accomplished with controls on the board itself.

11.2.4 Flyback Transformer

The flyback transformer is attached to the floor of
the tube enclosure. It is removed by performing the
following steps:

1. Remove the CRT by following the
    instructions in subsection 11.2.1.

2. Disconnect the flyback transformer cable
    from P3 on the video board.

3. Remove the flyback transformer cable from
    any cable tiedowns.

4. Remove the bottom panel of the cabinet by
    removing the six screws in the logic
    enclosure.

5. Remove the two nuts underneath the
    cabinet, taking care to hold the
    transformer to prevent it falling once
    these are removed.

When replacing the assembly, ensure that the HV lead
is to the back. Clip the bottom of the transformer
at the front first and follow the disassembly
procedure in the reverse order.

11.3 Cabling

Due to the modular nature of the logic electronics, the interconnections within the Lisa have been kept to a minimum. Interconnections fall into four categories:

* Power cabling
* Disk cabling
* Interface connections
* Logc connections.

11.3.1 Power Cabling

Power is supplied to the Lisa through a three-wire wall connector and a power cable to a socket in the power-supply assembly. The power-supply assembly in turn provides power to the Lisa via an edge connector, which mates into a plug in the CRT enclosure. The edge connector is part of the power cabling harness that distributes power to the following assemblies:

* Motherboard
* Video board
* Speaker
* Cover interlock.

Should it become necessary to remove the power harness, the procedure in subsection 11.2.1 must be followed to first remove the CRT. The following steps are then followed:

1. Remove the two screws that hold the video board connector to the wall of the CRT enclosure.

2. Remove the two screws that hold the power supply connector plug to the back wall of the CRT enclosure.

3. Disconnect the speaker plug on the floor of the CRT enclosure.

4. Remove the screw that holds the cover interlock to the cabinet beside the speaker.

5. Remove the two screws that hold the motherboard connector to the wall of the logic board enclosure.

6. Remove any tiedowns holding the cabling
    to the cabinet.

7. The harness can then be removed from the
    cabinet.

Installation of a power cable harness is performed
in the reverse order. Before installing any
tiedowns, ensure that the cable is correctly
positioned and that all connectors can reach their
proper locations.

If difficulty is encountered mounting the
motherboard connector, removal of the flyback
transformer makes this connector more accessible.

Ensure that the ground connectors are correctly
attached by one of the mounting screws for both the
power supply and the video board connectors.

11.3.2 Disk Cabling

The two floppy-disk drives are installed as a single
unit in the right-front of the cabinet. They are
connected to the logic by means of flat ribbon
cables, one for each drive. The cable also provides
the logic connection to the board that carries the
power switch and the keyboard phone jack at the
lower-right front of the cabinet.

To gain access to the cable, first remove the drive
assembly 620-5107. Then all steps called for in
subsection 11.2.1 must be performed to remove the
card cage, power supply and CRT. Finally, to remove
the disk cable:

1. Release the cable from the two tiedowns.

2. Unplug the connector to the switch board
    that contains the power switch and the
    keyboard jack.

3. Remove the two screws that hold the disk
    cable motherboard connector to the back
    of the logic enclosure wall.

Installation is performed in the reverse order.
Ensure that the cable has sufficient slack to allow
the drives to be placed in front of the cabinet with
the cable attached.

11.3.3 Interface Connections

Interface cabling in the Lisa consists of those
connectors at the back of the motherboard. No
disassambly procedure is required. It is however
recommended that connections are made and broken
with power off.

The interface connectors themselves are soldered to
the motherboard and are not separately replaceable.

11.3.4 Logic Connections

All logic cabling in the Lisa is made by means of
edge connectors between logic cards, with the
exception of the disk cable, described in subsection
11.3.2 above. There is therefore no disassembly
procedure.

11.4 Disk Drive Assembly

The disk drive assembly consists of the following
components:

* Drive carrier 805-4014
* Drive-carrier shelf 805-4013
* Upper-disk drive 653-6110
* Lower-disk drive 653-6110.

There is no difference between the upper and lower
drives. They are distinguished logically by the
connections made by the two plugs on the disk drive
cable.

To remove the bottom drive, remove the four 6-32
Phillips screws on the under surface of the assembly
and slide the drive out.

To remove the top drive, remove the six 6-32
Phillips screws that hold the drive carrier shelf in
the middle of the assembly, there are three on each
side. The shelf and top drive can then be slid out
of the assembly. The drive is detached by removal
of the four screws on the underside.

11.5 Miscellaneous

The following assemblies are present in the cabinet in
addition to those covered in the Lisa Owner's Guide and

the preceding sections. These are:

* Speaker assembly
* On-off switch assembly
* Motherboard assembly
* Cabinet assemblies.

11.5.1   Speaker Assembly

The speaker is located on the floor of the CRT
enclosure. In order to remove it, it is necessary
to remove the CRT, as described in subsection
11.2.1. Then the following procedure is followed:

1. Disconnect the speaker from the power
    cable harness by unplugging the plastic
    connector.

2. Remove the three screws holding the
    speaker to the cabinet.

3. Remove the speaker.

To install a speaker, follow the steps above in the
reverse order.

11.5.2   On-Off Switch Board Assembly

The on-off switch board is located on the
lower-right front of the cabinet. In order to
remove the on-off switch board, the disk drive
assembly must first be removed, as explained in
section 11.4. Then do the following:

1. Unplug the disk cable from the connector
    on the switch board.

2. Use a long-reach Phillips screwdriver to
    remove the two screws which hold the
    board to the base of the cabinet.

3. Remove the board.

Reassembly is performed in the reverse order.

11.5.3   Motherboard Assembly

The motherboard assembly is the carrier unit for all
the logic cards in the system. It consists of the

basic PCB with card edge connectors and interface
connectors attached plus card guides and a metal
frame.

The top of the expansion board card guides can be
removed by removing the three Phillips screws that
hold it to the top of the left-hand main card
guide.

The card guides can be detached by removing the six
4-40 Phillips screws that hold the main card guide
assembly in place. The two main card guides are
attached to one another by three support bars, each
of which is held at each end by a Phillips screw.

The metal motherboard frame can be detached from the
motherboard itself by removing the fifteen 4-40
Phillips screws that hold the two together. Eight
of the screws hold the interface connectors in
place. The other seven hold the motherboard to the
frame.

11.6   Keyboard and Mouse

The keyboard and mouse can be detached from the cabinet,
since they are physically separate elements. Also, both
may be disassembled if the need arises.

11.6.1   Keyboard Assembly

The keyboard consists of a single PCB which carries
all the keys sandwiched between two halves of the
case. To access the assembly:

1. Disconnect the keyboard from the Lisa by
    removing the keyboard jack from the plug
    at the lower-right of the cabinet.

2. Using a Phillips screwdriver, remove the
    five screws that hold the keyboard
    together.

3. Remove the keyboard PCB and place it on a
    flat surface.

Reassembly is performed in the reverse order. Care
must be taken not to apply excessive torque to the
threads of the screws.

The keyboard cable is held in place by a Molex-type
connector, which provides strain relief. This can

be removed as required.

11.6.2 Mouse Assembly

The mouse is a stand-alone device that has a few
moving parts. To access the mouse assembly, unplug
it from the back of the cabinet and remove the three
plastic screws on the underside that hold the body
together.

GLOSSARY

Acknowledge   A signal used during handshake
                   operations to indicate that the
                   current step has been completed.

AS   Abbreviation for address strobe;
                   <<which is ....>>.

Asserted   A signal in a true state, which means
                   that the term SIGNAL is in a "high"
                   or "1" state; the term SIGNAL/ is in
                   a "low" or "0" state if it is
                   asserted.

Asynchronous   A modem that handles asynchronous
modem   transmissions. In asynchronous
                   communication, each character is
                   transmitted with its own framing
                   information telling the receiver
                   where the character starts and
                   stops. Since each character is a
                   complete message, the time interval
                   between successive characters need
                   not be fixed.

Autovector   The jump to the interrupt handler
                   preloaded at a certain location.
                   When handling certain interrupts, the
                   68000 automatically jumps to a
                   location predefined for the given
                   interrupt.

Battery backup   The rechargeable Nickel/Cadmium
                   batteries with which the I/O board is
                   equipped. Whenever the Lisa is
                   disconnected from a power source, the
                   COPS device continues to receive
                   power from these batteries to allow
                   it to provide a true real-time clock
                   and also initiate software-controlled
                   power-up.

Baud rate   The rate at which a modem sends
                   and/or receives information. 110

	baud means the modem is handling approximately 11Ø bits per second. If there are two stop bits, a start bit, a parity bit, and a seven bit ASCII character code, 11Ø bits per second translates into about 1Ø characters per second.
BCD	Abbreviation for binary coded decimal; <<which is ....>>.
Bit	Acronym for binary digit; an item of data with only two possible states, either 1 (one) or Ø (zero).
B/L/	Abbreviation for base limit; <<which is ....>>.
Block	A contiguous set of data in the CPU; normally a unit of data written to and read from disk (524 bytes). When referring to memory, it may be of any length, but all addresses of the block are contiguous.
Booting	The process of getting the operating-system software into place and executing. When a computer is turned on, it must "bootstrap" itself into a useable state.
Buffer	A logic device used as a bus driver, whether it has latch capability or not.
Bus	A set of parallel wires, traces, and paths that carry related data and control information from one device to another.
Bus Timeout	A feature that permits the CPU to give peripherals a variable amount of time in which to respond to a transfer request. If the peripheral does not respond to a cycle after approximately 3Ø microseconds, a bus timeout occurs and the CPU logs an error.
Byte	A group of bits. On the Lisa, a byte is always 8 bits.
Byte parity	<<Is ....will someone define it concisely? Following is what the

	author provided>> When bytes of data are being moved around, one or more bits in the byte can get improperly flipped. These incorrect bits can sometimes be detected by checking the byte parity. The byte's parity is odd if there is an odd number of 1 bits in the byte. If another bit is available in the byte, the sender can ensure that every byte has even parity upon being transmitted. The receiver can then check each byte's parity, and if any are odd, it can inform the CPU that something has gone wrong.
Card cage	The metal frame that holds the printed circuit boards in the cabinet.
CAS	Abbreviation for column address strobe; <<which is ....>>
CASEN	Abbreviation for case enable; <<which is ....>>
Checksum	Similar to byte parity; a number used to ensure that data has not suffered degradation during transfer. A checksum is usually generated by addition of all the bytes in a block in a certain pattern. It is written at the end of blocks of data written to disk.
Clock	A continuous, regular waveform used to control the timing of logic decisions.
CMOS	Abbreviation for complementary metal-oxide semiconductor. CMOS combines N-channel and P-channel MOS transistors to give low power consumption. Since the non-volatile parameter memory must not consume much power, it is implemented with CMOS chips.
Context	A complete set of 128 pairs of registers within the MMU; the Lisa is configured to operate in one of four contexts. The operating system normally executes in context 0. Switching between programs can be

	quickly done by changing context.
COPS	Abbreviation for control-oriented processor system; in the Lisa, it is used as a controller at both ends of the keyboard interface.
Counter	A logic device that sequentially increments or decrements each time a clocking pulse occurs.
CPU	Abbreviation for central processing unit; the Motorola 68000 16-bit general-purpose device in the cabinet.
CRT	Abbreviation for cathode-ray tube; the screen inside the cabinet.
Cycle	The interval between the same phase position of two adjacent clock pulses.
Daisy chain	A method of connecting several devices to a single I/O port. Signal lines are passed from device to device in a chain.
Deasserted	A signal in a false state, which means that the term SIGNAL would be deasserted if it is "low" or "0"; the term SIGNAL/ is deasserted if it is "high" or "1".
Decode	Synonym of select. The decoder's input address determines which of its many outputs is asserted.
Disable	Holding any signal in a deasserted state, irrespective of other inputs.
DMA	Abbreviation for direct memory access; a device can read and write memory locations directly, without any intervention from the CPU. However, normal memory access goes through the 68000 and its memory manager.
Driver	A logic device capable of driving signals that have a large electrical load, such as occurs on a bus.
D/A	Abbreviation for digital to analog.

	When a digital signal is used to control an analog device, the bits in the digital word must be converted into analog voltage levels.
ECC	Abbreviation for error correction code; in memory, EEC is a way to regenerate erroneous data bits that occurr. Not yet implemented.
Edge detector	Logic that is capable of detecting a signal transition high-to-low or low-to-high.
Enable	Allow a signal to either respond to its gating inputs or to gate data into a further stage of the logic.
Expansion bus	The signal subset of the internal system bus that is made available on three card slots in the cabinet for the addition of other logic components.
Flag	A status bit that indicates the occurrence of some condition in the Lisa. It is usually available for interrogation by the CPU.
Flip flop	A digital circuit used to store one bit of data. There are variants on the basic theme but generally, the state changes synchronously with a clock edge, depending on the input state. Also known as "flop" and "FF".
Format	An exact description of the sequence of bits as they are organized on a disk.
Gate	A switch that controls the flow of data according to some Boolean function of its inputs.
GOBYTE	The flag byte used to tell the floppy-disk controller that the CPU wishes to have a macro instruction executed.
Handshake	The control of data-transfer between devices. Each device has a way to tell the other that its side of the operation is complete. For example,

	a processor writes data to a register, and then signals a device that data is ready to be read. The device reads the data, and then sends the processor a signal that it has finished reading and is ready for more. The handshake insures that the processor does not write new data to the register, thereby destroying the old data, before the device has had a chance to read the old data.
Hang	What happens to the computer when the CPU goes into an infinite loop or a wait state. If the operating system is unable to recover, your only recourse is to restart the machine.
Hard error	A non-recoverable error.
Header	The series of bytes at the beginning of a sector on a disk that identifies the sector.
Hexadecimal	The number system used within the Lisa. The digits in this base-16 system are 0-9 and A-F. All addresses and data are expressed in terms of hexadecimal numbers
High	A voltage state that can signify either true or false, depending on the logic being used.
Horizontal retrace	The period of time when the electron beam in the monitor is returning from the end of a line to begin the next.
KByte	Abbreviation for kilobyte; equal to 1,024 bytes.
KHz	Abbreviation for kilohertz; equal to 1,000 cycles per second.
Kword	Abbreviation for kiloword; equal to 1,024 words.
I/O	Abbreviation for input and/or output; a generic term that describes the peripheral system with which the CPU communicates with the outside world or with data storage other than main memory.

IOB	Abbreviation for I/O block; a block of memory used to control and communicate with the floppy-disk controller.
Interrupt	A signal that causes the CPU to suspend its current operation and ....
Latch	A register that contains data for a transient period of time; usually until read.
Logical Address	An expression that describes the address space generated by the CPU. Since logical addresses are translated into physical addresses by the MMU, these are not physical addresses. They can therefore remain constant even if physical addresses change, provided the MMU is informed of the change.
Low	A voltage state that can signify either true or false, depending on the logic being used.
LSB	Abbreviation for least significant bit; <<which is ....>>.
ma	Abbreviation for milliampere; equal to one-thousandth of an ampere.
Main memory	The RAM located on the memory boards in the cabinet. Main memory is used as storage by the CPU only, and can vary in size from 256 Kbytes to 2 Mbytes.
MALE	Abbreviation for memory address latch enable; <<which is ...>>.
Memory bus	The collection of signals that interface the memory boards with the processor board.
Map	The translation of one addressing system into another. In the Lisa, it describes the process of converting logical addresses into physical addresses.

Mask	A pattern of bits that controls the contents of a register. Mask bits need not be contiguous.
Matrix	The two-dimensional array of bits in memory.
Mbyte	Abbreviation for megabyte; equal to one million bytes.
MHz	Abbreviation for megahertz; equal to one million cycles per second.
mm	Abbreviation for millimeter; a unit of length equal to one-thousandth of a meter.
MMU	Abbreviation for memory management unit: hardware in the Lisa that provides a feature called relocation. This allows the CPU and, therefore, resident software to operate on logical addresses, which are translated into physical addresses by the MMU.
Motherboard	The circuit board whose main function is to provide connection between the other circuit boards.
Mouse	A detachable device that you can roll across a flat surface to direct cursor movement on the screen.
ms	Abbreviation for millisecond; equal to one-thousandth of a second.
MSB	Abbreviation for most significant bit; <<which is ...>>.
mV	Abbreviation for millivolt; equal to one-thousandth of a volt.
N-key rollover	Nearly all keyboard interfaces work by scanning the keys and forming a two-dimensional matrix representating the state of the keys. The logic involved can tell when two keys are being pressed simultaneously, rollover; however, when three or more keys are held down, phantom keys can appear. The N-key rollover design adds a diode in series with every key switch to eliminate hidden paths.

Nibble	A set of bits smaller than a byte. On the Lisa, a nibble is 4 bits.
NMI	Abbreviation for non-maskable interrupt. When the processor receives an interrupt, it usually checks a mask to see whether it should pass control to that interrupt's handler. A non-maskable interrupt is always honored.
ns	Abbreviation for nanosecond; equal to one-billionth of a second.
Oscillator	A device that provides an accurate time period. It is usually used in clock generation.
Page	Defines a contiguous area of main memory that is 512 bytes long. A logical page is this size of area within the CPU's logical address space. A physical page is this size of area within the main memory.
Parameter memory	A non-volatile block of RAM set aside for such things as the system serial number, configuration data, and user-defined information.
Parity	A function of the number of bits in a word that are high. If there are an even number, the word has even parity. Parity can be checked to insure that one bit in a word has not been incorrectly flipped during transmission.
PC	Abbreviation for program counter. A register within the CPU that keeps track of the next instruction to be executed after the current one is complete.
PIA	Abbreviation for peripheral interface adapter; an LSI logic device that assists the CPU in interfacing to peripheral logic. On the Lisa, Motorola 6522 VIA devices are used.
Pixel	The smallest controllable unit of area on the CRT. It corresponds to one bit of video data and can only be

on or off, black or white.

Port   An I/O address location within I/O space. In general, any group of addresses within the same PIA is termed a port also.

PROM   Abbreviation for programmable read-only memory; it refers to the fact that the ROM can be programmed. It is usually not-alterable while it is in a computer.

RAM   Abbreviation for random-acccess memory; it is read/write memory.

Recalibrate   A technique of establishing absolute track position of the disk heads returning to a known position.

Refresh   The operation whereby the dynamic RAM's used for data storage are refreshed with the data they contain.

Relocation   The technique implemented in MMU to map the logical address space used by the CPU into the physical address space that reflects the actual configuration of the Lisa.

Retry   Repeat the execution of an instruction or routine in an attempt to avoid an error result. Used most frequently on disk access.

ROM   Abbreviation for read-only memory; devices that are fabricated with an unalterable program already present.

RS232-C   An interface standard that defines a bit-serial interface for use in conjunction with a modem, plus a corresponding communication protocol.

RTC   Abbreviation for real-time clock; it is a function implemented on I/O board by the COPS device. Since power is always available to this device, it is used to calculate the real elapsed time at all times. This is available to software for interrogation.

RWTS		Abbreviation for Read/Write/Track/Sector; it refers to the controlling routines that drive the floppy disk. The RWTS is that part of the floppy-disk controller's resident program that interrupts the CPU upon completion since it involves actual disk control.
Sector		The smallest addressable portion of a disk. Each track normally contains several segments.
Seek		To move the heads across the disk surface to position them above a particular track.
Segment		An area of the system-address space. It is the main unit of memory dealt with by the MMU. A logical segment is a contiguous block of 128 Kbytes in the CPU's logical address space. It consists of 256 logical pages. A physical segment consists of between 1 and 256 physical pages, depending on the size allocated to it by software via the MMU. Each logical segment has a corresponding physical segment. There are 128 of each in a Lisa.
Sense		The operation of interrogating status.
Shared Memory		An area of memory that can be accessed by more than one processor. In a Lisa, the disk controller storage area is shared between the 6504 and the CPU.
Slot		One of the three slots in the cabinet available for peripheral boards.
SLR	.	Abbreviation for segment limit register; one of the registers within the four sets of 128 such registers contained in the MMU. It is used to define both the size of the physical segment being accessed in one page increments and the type of storage being accessed.
SOR		Abbreviation for segment origin

	register; one of the registers within the four sets of 128 such registers contained in the MMU. It is used to define the lowest address of the physical segment being accessed in terms of pages from the lowest address in memory.
State Machine	A collection of logic devices capable of executing a very simple series of steps sequentially. It is the simplest form of computer.
Status	An array of bits that is available to the CPU to inform it of the state of certain portions of the Lisa.
Strobe	A signal that indicates that data is being transferred for the time that the strobe signal is asserted.
Sync	A synchronization signal that permits other signals to assume a known state at a known time.
Synchronous modem	A modem that transmits synchronously, which puts the framing information around a group of characters. The transmitter then automatically inserts fill characters into the stream whenever necessary to maintain synchronicity. Because more of the bits are data, there are fewer stop and start bits than in asynchronous transmission, data transfers can go at a faster rate.
System Bus	The main bus, which is used to communicate between the processor and I/O boards. A subset of it extends to the expansion slots and is called the expansion bus.
Tristate	A logic output that can be inactive, asserted or deasserted. These three states may also be termed active high, active low, and open.
TTL	Abbreviation for Transistor-Transistor Logic; the most common kind of digital device in the Lisa.
Vertical retrace	The period of time during which the

	electron beam in the monitor is returned from the bottom of the screen to the top.
VIA	Abbreviation for Versatile Interface Adapter; the name used by Motorola for their 6522 peripheral port control devices.
Video	Of or pertaining to the CRT and its control circuitry.
Word	A group of bytes. On the Lisa, a word is usually 16 bits, or two bytes.
Write Protect	An operation that inhibits any writing operation to the item protected. This technique can be used for both memory and disks.
Yoke	The control windings on the CRT that deflect the beam.
ZIF	Abbreviation for zero insertion force, which refers to the type of connectors used for the three expansion slots in the cabinet. Since the slots are accessed from the side, a locking device is used to open the connector and permit the PCB's to be slid in from the side of the connector before being locked in place.

Appendix H. Alternate Keyboard Layouts

Following Lisa keyboard layouts are available in addition to
the standard, North American, layout shown in Chapter 8.

H-1

Spanish Keyboard Layout

LEGEND

		Left:	Right:
		Primary keyboard	Alternate keyboard

Upper: Shifted

Lower: Unshifted

BoldFace indicates that the character is printed on the keytop.

When no character is shown in the lower area of the keytop, one of the following is true:

a. If the symbol ⇩ is shown, the lower character is the lower case equivalent of the upper character.

b. If the symbol ⇩ is not shown, the lower character is the same as the upper character.

Left	Right
Up	Down
Horizontal Tab	
Caps Lock	
Shift	
Alternate Keyboard	
Command	
Back Space	
Return (New Line)	
Enter	
Clear	

▒ Character has lower case and is affected by Caps Lock.

▒ Dead key, no character is generated until next key is pressed.

US DVORAK Keyboard Layout
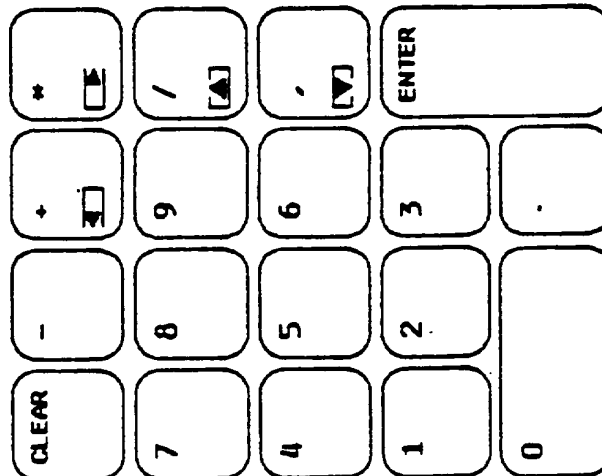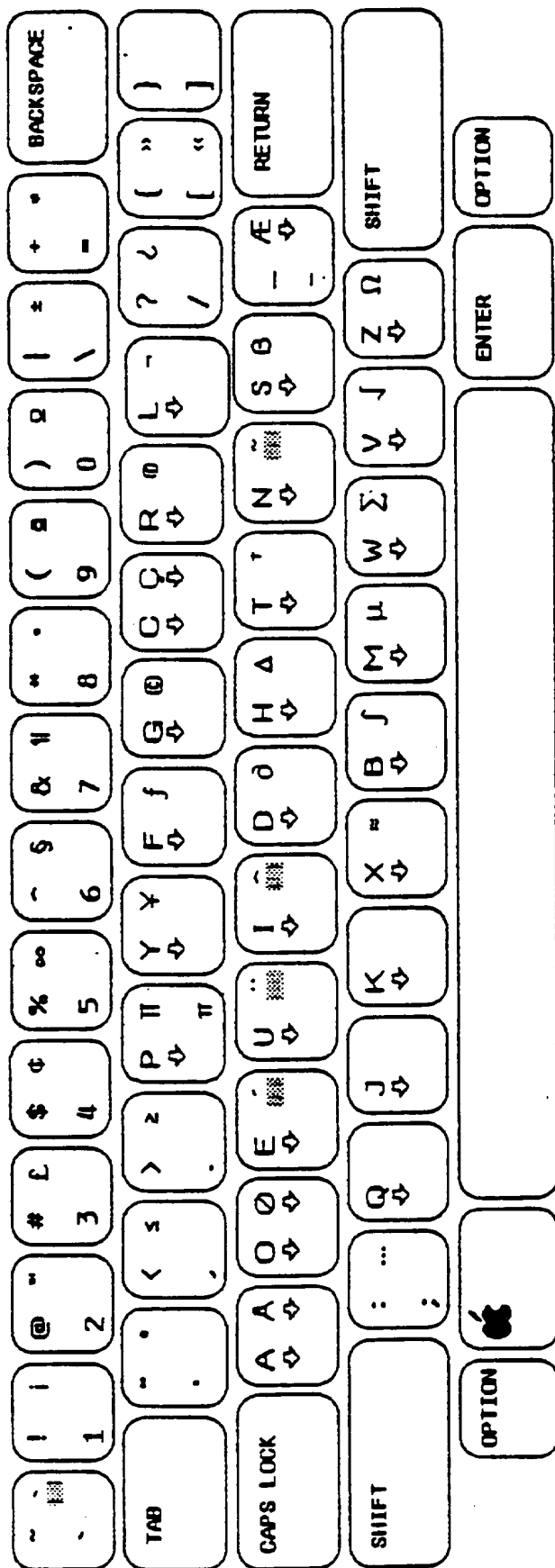
TN / 8 Nov, 82

LEGEND

◄⌐ Left
◄► Right
◄▲ Up
◄▼ Down

▓ Dead key, no character is generated until next key is pressed.

⇧ Character has lower case and is affected by Caps Lock.

OPTION Selects Alternate Keyboard

Left: | Right:
Primary Keyboard | Alternate keyboard

Upper: Shifted
Lower: Unshifted

BoldFace indicates that the character is printed on the keytop.

When no character is shown in the lower area of the keytop, one of the following is true:

a. If the symbol ⇧ is shown, the lower character is the lower case equivalent of the upper character.

b. If the symbol ⇧ is not shown, the lower character is the same as the upper character.

UK Keyboard Layout

TN / 8 Nov, 82

LEGEND

	Left:	Right:
	Primary keyboard	Alternate keyboard

BoldFace indicates that the character is printed on the keytop.

When no character is shown in the lower area of the keytop, one of the following is true:

a. If the symbol ⇩ is shown, the lower case character is the lower case equivalent of the upper character.

b. If the symbol ⇩ is not shown, the lower character is the same as the upper character.

⬛ Left

⬛ Up

⬛ Right

⬛ Down

↦ Horizontal Tab

⇧ Caps Lock

⇧ Shift

⇩ Alternate Keyboard

Command

↤ Back Space

Return (New Line)

Enter

Clear

Character has lower case and is affected by Caps Lock.

Dead key, no character is generated until next key is pressed.

Italian Keyboard Layout

TN / 12 Nov, 82

LEGEND

Left: Left: | Right:
Primary keyboard | Alternate keyboard

Upper: Shifted

Lower: Unshifted

BoldFace indicates that the character is printed on the keytop.

When no character is shown in the lower area of the keytop, one of the following is true:

a. If the symbol ⇨ is shown, the lower character is the lower case equivalent of the upper character.

b. If the symbol ⇨ is not shown, the lower character is the same as the upper character.

| | Left | | Right |
| | Up | | Down |
Horizontal Tab
⇨ Caps Lock
⇦ Shift
Alternate Keyboard
 Command
Back Space
Return (New Line)
Enter
Clear

Character has lower case and is affected by Caps Lock.

Dead key, no character is generated until next key is pressed.

Swedish Keyboard Layout

TN / 8 Nov 82

LEGEND

Left: | Right:
Primary keyboard | Alternate keyboard
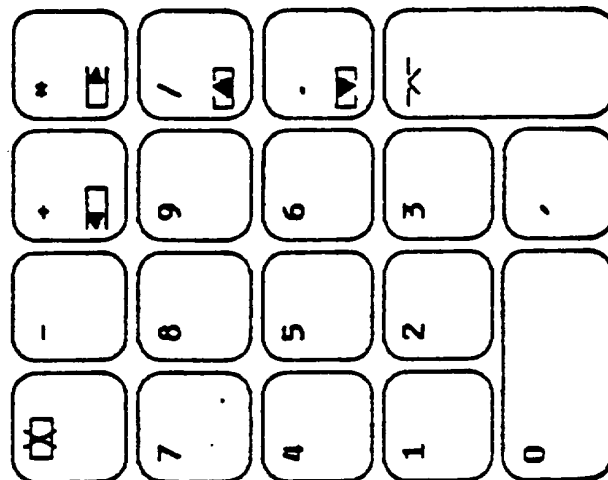
Upper: Shifted
Lower: Unshifted

Boldface indicates that the character is printed on the keytop.

When no character is shown in the lower area of the keytop, one of the following is true:

a. If the symbol ⇩ is shown, the lower character is the lower case equivalent of the upper character.

b. If the symbol ⇩ is not shown, the lower character is the same as the upper character.

Left
Up
Horizontal Tab
Caps Lock
Shift
Alternate Keyboard
Command
Back Space
Return (New Line)
Enter
Clear
Character has lower case and is affected by Caps Lock.
Dead key, no character is generated until next key is pressed.

Right
Down

German Keyboard Layout

TN / 8 Nov, 82

LEGEND

Left: | Right:
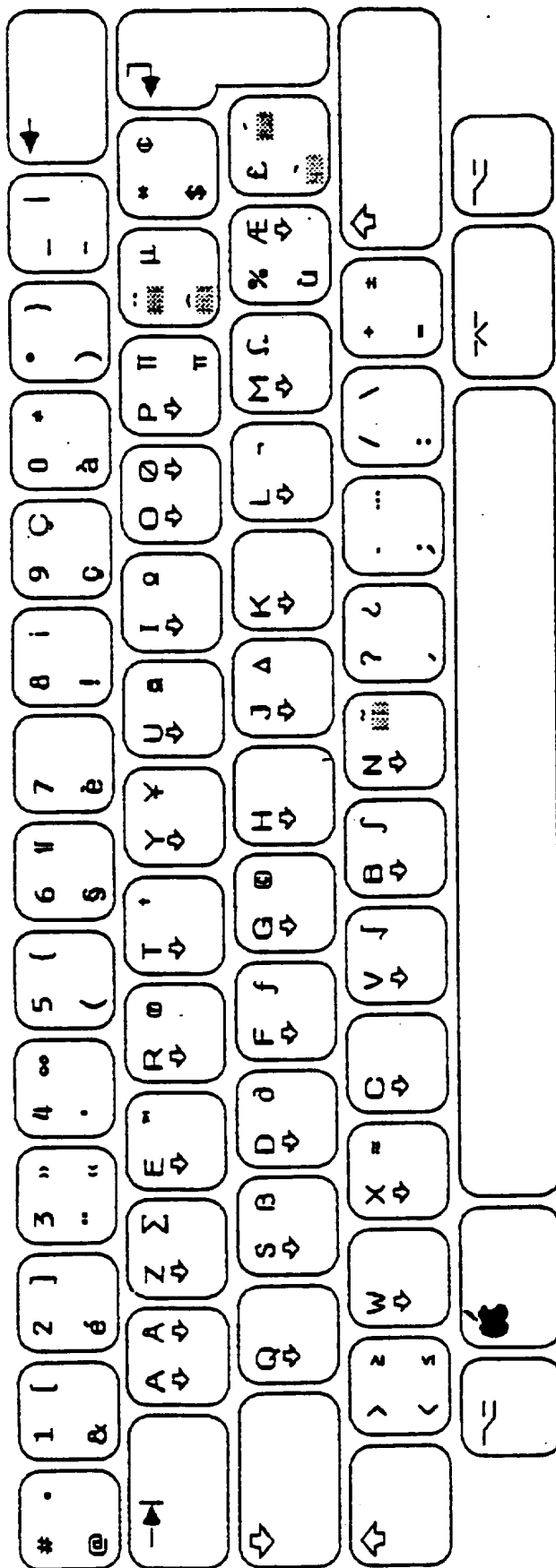Primary keyboard | Alternate keyboard

Boldface indicates that the character is printed on the keytop.

When no character is shown in the lower area of the keytop, one of the following is true:

a. If the symbol ⇩ is shown, the lower character is the lower case equivalent of the upper character.

b. If the symbol ⇩ is not shown, the lower character is the same as the upper character.

P ⇩ | π
π | Upper: Shifted
 | Lower: Unshifted

⊡ Left   ⊡E Right
⊡ Up   ⊡ Down
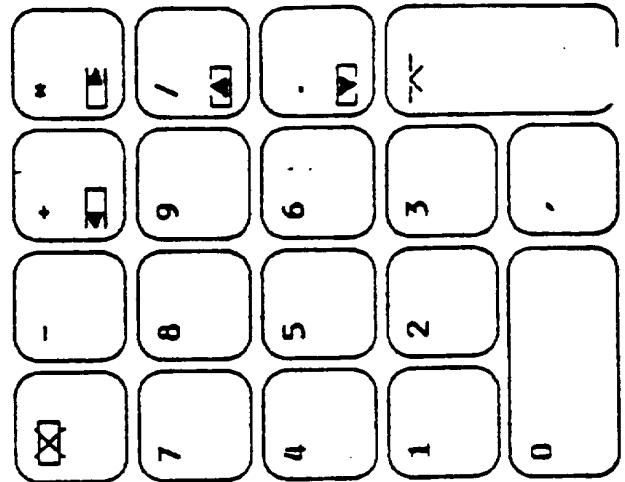Horizontal Tab
Caps Lock
Shift
Alternate Keyboard
Command
Back Space
Return (New Line)
Enter
Clear

Character has lower case and is affected by Caps Lock.

Dead key, no character is generated until next key is pressed.

French Keyboard Layout

TN / 8 Nov, 82

LEGEND

Left: | Right:
Primary keyboard | Alternate keyboard

P Π   Upper: Shifted
π   Lower: Unshifted

BoldFace indicates that the character is printed on the keytop.

When no character is shown in the lower area of the keytop, one of the following is true:

a. If the symbol ⇨ is shown, the lower character is the lower case equivalent of the upper character.

b. If the symbol ⇨ is not shown, the lower character is the same as the upper character.

Left
Up
Right
Down
Horizontal Tab
Caps Lock
Shift
Alternate Keyboard
Command
Back Space
Return (New Line)
Enter
Clear
Character has lower case and is affected by Caps Lock.

Dead key, no character is generated until next key is pressed.

Lisa Theory of Operations Appendix

Appendix J. Radio and Television Interference

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The Lisa generates and uses radio frequency energy. If the
Lisa is not installed and used properly (that is, in strict
accordance with these instructions), it may cause interference
to radio and television reception.

This equipment has been tested and complies with the limits
for a Class B computing device in accordance with the
specifications in Subpart J of Part 15 of FCC rules. These
rules are designed to provide reasonable protection against
such interference in a residential installation. However,
there is no guarantee that the interference will not occur in
a particular installation, especially if a "rabbit ear" TV
antenna is used. (A rabbit ear antenna is the telescoping rod
antenna usually contained on TV receivers.

You can determine whether your computer is causing
interference by turning it off. If the interference stops, it
was probably caused by the computer or its peripherals. To
further isolate the problem:

o Disconnect the peripheral devices and their I/O
   cables one at a time. If the interference stops, it
   is caused by either the peripheral or its I/O cable.
   These devices usually require shielded I/O cables.
   For Apple peripherals, you can obtain the proper
   shielded cable from your dealer. For non-Apple
   peripherals, contact the manufacturer or your dealer
   for assistance.

If your computer does cause interference to radio or
television reception, you can try to correct the interference
by using one or more of the following measures:

o Turn the TV or radio antenna until the interference
   stops.

o Move the computer to one side or the other of the TV
   or radio.

o Move the computer farther away from the TV or radio.

o Plug the computer into an outlet that is on a
   different circuit from the TV or radio. That is,

J-1

Lisa Theory of Operations Appendix

make certain the computer and the TV or radio are on circuits controlled by different circuit breakers or fuses.

o Consider installing a rooftop TV antenna with coaxial cable lead-in between the antenna and the TV.

If necessary, you should consult your dealer or an experienced radio/television technician for additional suggestions. You may find helpful the following booklet, prepared by the Federal Communications Commission: How to Identify and Resolve Radio-TV Interference Problems. This booklet is available from the U.S. Government Printing Office, Washington, D.C. 20402, Stock Number 004-000-003454.

FINIS

J-2